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A Preamp-ADC Interface Amplifier For The BaBar Drift Chamber

1 Introduction and Requirements

The amplifier described in this note is intended to interface an existing preamplifier chip under development by D. Dorfan and N. Spencer at UCSC with a conventional ADC module. The preamp chip provides differential-voltage-mode outputs capable of driving 50-Ω loads. However, the differential channels are made up of emitter-followers with approximately $4V_{\mathrm{be}}$ of voltage difference under zero signal conditions. Thus, to first approximation one side of the output will have a quiescent level near 4 volts and a negative signal swing. The other output will have a quiescent level near 1 volt and a positive signal swing. Both channels should be used together to preserve as much power-supply noise rejection as possible.

Several conventional ADC chips can be used to provide the dE/dx measurement for the Drift Chamber. The useful dynamic range of the data has been estimated by D. Coupal to be approximately six bits, while a sample rate of 15 MHz in view of the several-hundred-nsec drift time. Conventional ADC units such as the eight-bit Analog Devices AD775 will easily meet these requirements. A six-bit device under development by LBL is also considered a potential candidate. Both of these devices are single-ended. The input signal range of the LBL FADC part is 1-4 volts and is expected to require an interface to the preamp with a gain of two. The full-scale range of the AD775 is two volts peak to peak and will probably not require any gain in the interface. The final gain selection of the preamp-ADC interface amplifier has not been made, but for the purposes of this report a gain of two will be assumed. Finally, since the ADC data may be subject to pile up, an ac-coupled interface should be avoided.

2 Discussion

The proposed interface amplifier schematic is shown in Figure 1. The configuration is a conventional differential-to-single-ended circuit. The node V_{offset} in conventional applications of the circuit is usually grounded. However, in this application the node voltage V_{offset} will be raised to about 4 volts to provide a pedestal offset and to cancel the $4V_{\text{be}}$ voltage difference noted earlier. The nominal differential gain of the amplifier is two for $R1 = R2$. The quiescent voltage of the output, V_{out}, will be about 1 volt. The amplifier does not provide any shaping and can use any conventional op-amp with a suitable gain-bandwidth product. The Analog Devices OP-467 ($1.65 per channel, 25 mW per channel) provides four amplifiers per package and is a good selection. A nominal resistor value of $R1 = R2 = 1\ \text{k}\Omega$ is suitable for a discrete implementation.

An integrated-circuit version would likely benefit from a higher resistor value in the range of 2-5 kΩ to reduce on-chip heating. The basic circuit design is relatively process independent and could be fabricated as part of the Maxim bipolar process used for the preamp or as a CMOS device, provided the process supports a nominal poly-sheet resistance of 30 $\Omega/\square$ to limit the required size of the resistors and provide matching of the various resistor ratios. Unfortunately, for the moment, the prototype bipolar preamp design uses all of the parts available and the 0.8-micron Mosis CMOS process selected by LBL provides sheet-resistance values less than 5 $\Omega/\square$. This low value of sheet resistance will lead to large area resistors. A preliminary estimate of the required area is 0.25 mm^2.

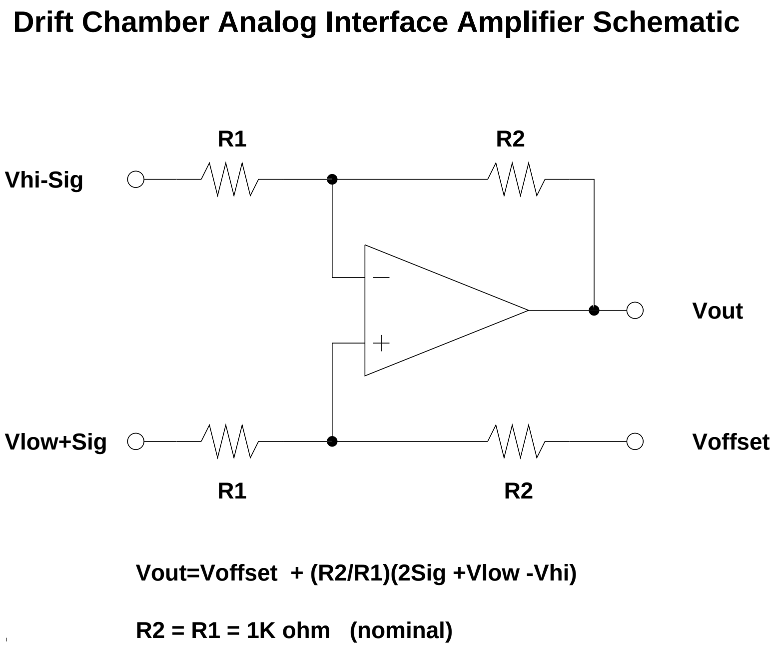

Figure 1: Basic preamp-ADC interface amplifier.

3 A Discrete dE/dx Suggestion

The potential use of a discrete interface circuit, such as that described above, prompts us to review the overall processing task to see if it is feasible to implement most or all of the remaining required functions using commercially available devices. The functions to be performed include:

1. ADC conversion at 6 bits (or more) dynamic range and 15-MHz sample rate;
2. Storage of the ADC results for 12 μsec pending Level-1 accept (*i.e.*, 180 samples);
3. Storage of, say, 4 Level-1 accepts of 2-μsec duration each (*i.e.*, 120 samples); and finally a parallel-to-serial converter to simplify final readout of the accepted sample sets.

The 2-μsec duration per event is composed of 1 μsec of transit-time spread in the drift chamber and 1 μsec of trigger jitter.

The required functions can be implemented using commercially available devices as shown in Figure 2. The ADC function is performed using one AD775 converter per wire ($10 ea., 60 mW). The Level-1 fifo and the Output fifo buffers can be implemented using a pair of fifo chips such as the IDT7200 ($3.20 ea., 250 mW). The parallel-to-serial shift register circuitry, based on a CD4021 chip ($0.50 ea., 30 mW at 15 MHz), is straightforward, but an essential factor in a successful system design.

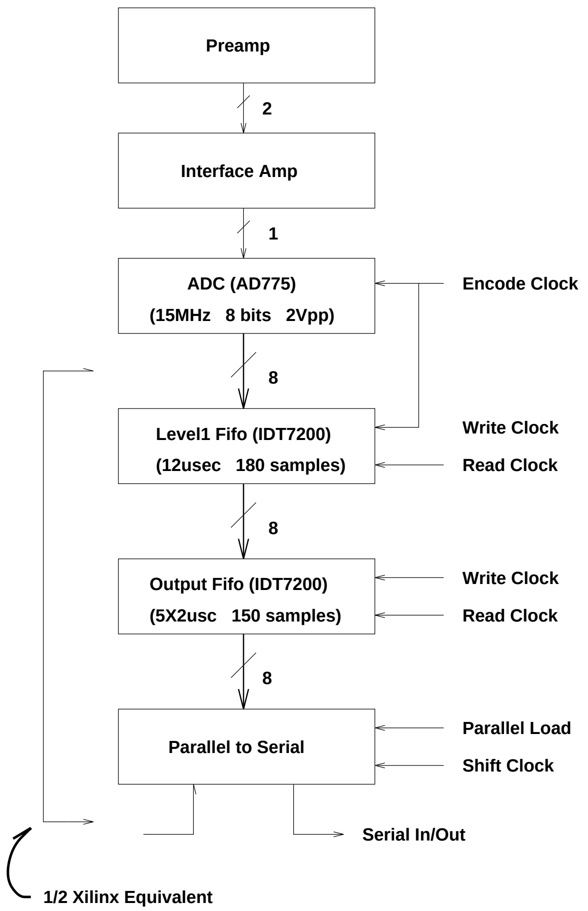

Figure 2: Single-channel dE/dx readout block diagram.

In operation, the ADC would encode data continuously using a subharmonic of the system clock near 15 MHz. Writing of encoded ADC data into the Level-1 fifo would also be done continuously at the same rate using the same clock. After an initial startup delay of 180 8-bit samples to establish the 12-μsec buffer depth, the output read clock for the Level-1 fifo always proceeds in step with the write clock. By reading out one sample each time a new ADC sample is written into the Level-1 fifo, the Level-1 delay is maintained at 12 μsec. The IDT7200 part has a total fifo depth of 256 samples. The part would therefore be able to provide up to 17 μsec of Level-1 delay, or any shorter value, under global Drift Chamber control. Sample values read out from the Level-1 fifo are lost in the absence of a Level-1-Accept signal.

Upon the arrival of the Level-1-Accept signal the data read out from the Level-1 fifo are immediately written into the Output fifo. Writing data into the Output fifo continues at the rate of 15-MHz until the 30 samples associated with an event have been transferred, *i.e.*, for a total of 2 μsec. The size of the data set associated with a Level-1 Accept can be changed under global control by changing the total number of Output-fifo write signals issued.

Readout of the Output fifo is controlled by the subsystem DAQ. The required size of the Output fifo depends the average rate of arrival of the Level-1-Accept signals and the DAQ readout rate. The IDT7200 part can store 256 bytes, or eight 30-sample data sets. This level of storage is probably realistic, but can be increased to 16 kbytes without changing the pin count or package size. The fluctuations in the expected number of samples in the output buffer can be approximated using a Poisson distribution

$$\sum_{j=0}^{c} P(m,j) = \sum_{j=0}^{c} \frac{e^{-m} m^j}{j!}$$

This relation can be used to predict how frequently we should expect more than c Level-1 events will occur during the normalized time interval m. The time interval m is scaled such that $m = 1$ represents an expectation that an average of one Level-1 event will occur during the average readout period for a single event. Values of $m < 1$ represent either lower average rates of Level-1 or shorter readout times. Values of $m > 1$ represent conditions in which the readout system cannot keep up with the average level-1 rate.

The basic probability model can be expanded to account for series of readout periods with various combinations of events occuring during each period such that the buffer overflows during the last period. The calculation is straightforward but very tedious.[1] For purposes of preliminary sizing of the buffer we will assume a slightly optimistic two period model in which the buffer is empty at the begining of the first period and overflows during the second period and a high average acceptance rate of $m = 1$. The expect overflow rate is summarized in Table 1.

The Table indicates that a buffer length of 4-5 should be adequate for preliminary design purposes. A more detailed analysis can be done when final parameters of the DAQ design are available.

The serial readout of the Output Fifo using a 15-MHz shift clock would, in principle, support an average Level-1 accept rate of 60 kHz. At this performance level it is practical to

[1] See Princeton/BABAR/TNDC-96-44.

c	$P_{overflow}$
4	0.044
5	0.016
6	0.004

Table 1: Probability that a buffer of length c will overflow during the second readout period, assuming the buffer is empty at the begining of the first readout period and an average of occurence of one level-1 event per readout period.

consider daisy chaining together several serial outputs from adjacent channels to minimize the system level readout wiring.

The architecture proposed above is relatively easy to implement using off-detector rack mounted electronics, but requires 1 watt per channel which is considered rather high for electrnics mounted on the drift chamber endplate. However, the design can be can be simplified and the power reduced by the using field programmable gate arrays (FPGAs) such as the Xilinx 4005A. This type of device provides sufficient random access memory (RAM) to implement enough fifos for the readout of two sense wires. Using internally decoded RAM to implement the fifo functions avoids shifting data in the device and minimizes device power consumption. Using the Xilinx routing and logic resources can also be expected to reduce the overall footprint area of the readout circuit.

Initial development of prototype hardware can proceed using serial data lines to load the Xilinx device logic pattern. Fabrication of fixed logic pattern devices in production quantities can be done using commercially available foundry services such as the Encore service offered by Orbit Semiconductor Inc.

The proposed single-channel readout is controlled by 5-6 global signal lines depending on the details of the subsystem data readout. A dual-channel readout circuit for two sense wires, implemented using FPGAs consists of four integrated circuits, eight resistors and six to 10 bypass capacitors. This appears to fit within the 2.5 cm^2 area per channel on the endplate envelope if 10-15 cm are available normal to the endplate. Some additional packing efficiency can be expected from the use of quad op-amp devices and possibly from recording only seven of the eight ADC bits. The need for an additional dE/dx trigger can be implemented using an additional dual comparator chip.

The relative simplicity of the above discrete dE/dx implementation is encouraging and suggests pursuing a more detailed layout to verify that the packaging, power and signal-routing and interface issues can be resolved.