Progress Report and Renewal Request for R&D on

A Silicon Vertex Detector with Interleaved Disks and Barrels

(Submitted to the Superconducting Super Collider Laboratory)

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Summary

For a B-physics experiment at a hadron collider, the large angular range of the B-decay products leads to the requirement of a silicon vertex detector with interleaved disk and barrel detectors. As no present or approved collider experiment uses this geometry we have undertaken an R&D program to demonstrate its viability. We report on progress on mechanical modelling, development of custom VLSI readout chips, bench and beam tests of silicon detectors, and on simulations of system performance. We propose a two-year continuation of this program to produce two hexagonal modules of fully instrumented silicon detectors. For this we seek a budget of **$287k** at U. Oklahoma and **$135k** at Princeton U., with 50% of the funding in each of FY92 and FY93.

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1 Introduction

A B-physics experiment at the SSC would be an excellent extension of the Higgs-sector program already underway via SDC and GEM. We have presented a preliminary vision of such an experiment in EOI0008 [1, 2].

The critical component of a B-physics detector is the silicon vertex detector. For an experiment at the SSC collider the vertex detector should cover a large rapidity range to maximize the acceptance of the low-transverse-momentum B's. Present collider detectors (CDF, MarkII, ALEPH, DELPHI, OPAL) all have vertex detectors with a 'barrel' configuration matched to the central rapidity region. Fixed-target experiments all have planar detector configurations. The best option for a collider B-physics experiment is, we believe, a configuration of interleaved 'barrels' and planar 'disks' of silicon detectors. We expand on this view in Sec. 1.1 below.

No presently approved experiment anywhere plans to use such a configuration. Hence if the community is to be convinced of its viability, a demonstration must be made as a new R&D effort. The BCD collaboration has been engaged in first steps in such an R&D program since 1989 [3, 4, 5, 6, 7], but the results are not yet definitive. Here we propose a program to complete the demonstration of a prototype barrel and disk module in two years, so as to influence in a timely manner the possible inauguration of a B-physics program at the SSC.

1.1 The Need for Interleaved Barrels and Disks

The silicon vertex detector must locate the secondary vertex of the B's ($c\tau \approx 360$ μm) to isolate the B-decay products from the high-multiplicity primary event. The broad range of angles of the B-decay products leads to the need for a complicated configuration of the vertex detector. If we only desired to observe tracks at small angles to the beams we would use an array of 'disks' as sketched in Fig. 1a, while for large angles a 'barrel' array (Fig. 1b) would be ideal. However, we cannot build a large-solid-angle vertex detector out of separate disk and barrel modules for two reasons:

1. The finite length of the luminous region blurs the correlation between a silicon detector's position and its angle from the primary vertex, as shown in Fig. 2. Hence the barrel detectors must extend over a length roughly that of the luminous region.

2. The vertex resolution of both disk and barrel detectors is determined by the radius at which the first measurement is made, as discussed in the following paragraph. (This result contrasts with the use of the detectors for momentum measurement, where the total path length observed is the critical parameter.) Hence the disk detectors cannot be backed off to make room for the enlarged barrel detector without sacrificing vertex resolution.

   We illustrate the claim in the preceding paragraph with a simplified calculation of vertex resolution. Suppose the vertex detector consists of only two disks, at z_1 and z_2. From measurements of coordinates r_1 and r_2 we extrapolate a straight-line fit back to $z = 0$ and use $r(0)$ as the measure of fit to the primary vertex. Each of

Figure 1: **a)** A simple vertex detector consisting of two 'disk' detectors. The measurement of coordinate r_2 in the second detector is subject to an uncertainty caused by multiple scattering in the first detector. Both detectors have the same intrinsic measurement uncertainty. The intercept at $z = 0$ of the straight-line fit from the two data points is a measure of how well the track fits to the primary vertex. **b)** A vertex detector consisting of two 'barrel' detectors.

r_1 and r_2 are subject to a measurement uncertainty $\sigma_{\rm meas}$, and r_2 is subject to an additional uncertainty due to the multiple scattering caused by detector 1. Since $r_2 = r_1 + (z_2 - z_1)\tan\theta$, the effect of multiple scattering is

$$\sigma_{\rm M.S.} = \frac{(z_2 - z_1)\sigma_\theta}{\cos^2\theta} \approx \frac{(z_2 - z_1)0.015\sqrt{T}}{P[{\rm GeV}/c]\cos^{5/2}\theta} \approx 10[\mu{\rm m}]\frac{(z_2 - z_1)[{\rm cm}]}{P[{\rm GeV}/c]\cos^{5/2}\theta},$$

for a silicon wafer of thickness $T = 300$ μm. The intercept of the straight-line fit is

$$r(0) = \frac{r_1 z_2 - r_2 z_1}{z_2 - z_1},$$

so the uncertainty in this is

$$\sigma_{r(0)} = \frac{\sqrt{z_2^2\sigma_{r_1}^2 + z_1^2\sigma_{r_2}^2}}{z_2 - z_1} = \frac{\sqrt{(z_2^2 + z_1^2)\sigma_{\rm meas}^2 + z_1^2\sigma_{\rm M.S.}^2}}{z_2 - z_1}.$$

Now $z_1 = r_1/\tan\theta$, and typically $z_2 = 2z_1$, so we have

$$\sigma_{r(0)} \approx \sqrt{5\sigma_{\rm meas}^2 + \left(\frac{10[\mu{\rm m}]r_1[{\rm cm}]}{P_t[{\rm GeV}/c]\cos^{3/2}\theta}\right)^2}.$$

We expect $\sigma_{\rm meas}$ to be about 5-10 μm, so for P_t of order 1 GeV/c we would like r_1 only 1 cm or so. Then we could achieve $\sigma_{r(0)} \approx$ 20-30 μm $\approx c\tau_B/15$.

A very similar argument can be made for vertexing in a barrel detector, in which detector elements at radii r_1 and r_2 measure coordinates z_1 and z_2. The uncertainty

Figure 2: A vertex detector with separate disk and barrel silicon does not give optimal angular coverage if the luminous region has a finite extent.

in the extrapolated value $z(0)$ has the same form as that just found for $\sigma_{r(0)}$ but with the $\cos^{3/2}\theta$ changed to $\sin^{3/2}\theta$. Hence both disk and barrel detectors must begin at very small radii.

We conclude that it is vital to build a vertex detector with interpenetrating regions of disks and barrels if both large- and small-angle tracks are to be analyzed.

2 Progress Report

Besides the authors of the present document, our R&D program involves collaborators from Fermilab, IIT, and ORNL. In this Section we review all facets of our silicon detector R&D. The specific proposal for new work to be supported by the SSC Subsystem R&D Program is given in Sec. 3.

The silicon vertex detector for a hadron collider is, by necessity, ambitious and complex. The basic design criteria have already been discussed in the introduction. Considerations of full acceptance (roughly ± 4 units of pseudorapidity), low mass, and the finite size of the interaction region lead to a device 3-4 m long, 10-20 cm in radius, and containing 1-2 square meters of double-sided AC-coupled silicon detectors. A spatial accuracy of 5-7 μm for angles of incidence up to 60° on the detector requires detectors of strip pitch 25-50 μm and digitization of the signals, which can only be accomplished in a cost-effective manner with on-detector VLSI chips with ambitious specifications. This detector will have in excess of 1 million channels distributed over ~ 1000 wafers.

There have been several iterations of the vertex detector concept, starting with a design which placed the silicon detectors inside of the vacuum pipe, which was largely the work of P.

Karchin [8]. This arrangement was superceded by the proposal of Kalbfleisch and McDonald [9] and further refined by Karchin, Kalbfleisch, and McDonald into the present model of discs and barrels located outside the vacuum pipe.

The structure of the current vertex detector conceptual design is shown in Fig. 3 and consists of self-supporting silicon modules housed in one rigid external beryllium tube. All modules have the same mechanical structure. In the central region both the barrel and disk areas are active: in the forward region only the disk sections are instrumented. This design contains no ladders for support of the silicon detectors or readout chips. It relies on the structural integrity of the silicon wafers for internal alignment and uses the tube to align individual modules with respect to each other. The placement of the preamplifier chips directly on the silicon detector and the strip directions are indicated in Figs. 4 and 5. The stripe orientation was chosen for ease of preamplifier placement.

Figure 3: The BCD vertex detector with a cutout of the 'gutter' to show the self-supporting silicon modules inside.

The BCD vertex detector design contains three features not present in other existing or proposed collider vertex detectors.

1. The device is very long, roughly 3 meters along the beam axis. This length is necessary to provide vertex coverage over $\pm\eta = 4$.

2. The central rapidity region is a complex self-supporting structure composed of silicon barrels and disks extending over roughly $\pm 2\sigma_z$, where σ_z is the r.m.s. length of the luminous interaction region. This design permits vertex capability for tracks of all angles. A shorter interaction region would reduce the length of the detector and would

Figure 4: A representation of a single module of the Central portion of the vertex detector shown in Fig. 3. Disk and barrel silicon detectors are glued together into a hexagonal structure. The disks are mounted in a helicoidal pattern to allow a net longitudinal air flow through the detector for cooling. The stripes on the disk detectors are aligned along u and v axes which permits the readout chips to be placed at the outer edges only. The inner radius of the silicon is 1.5 cm, and the outer is 10 cm. Each module is 4.8 cm long.

therefore simplify the design. One consequence of the long design is that an equally long support structure is needed. This structure must bear the load of all the modules and yet be composed of a thin, low-Z material to minimize multiple-scattering effects. The proposed structure is a beryllium cylindrical tube, 10-20 cm in radius and is called a **gutter**.

3. The vertex detector will contain more than 1 million readout channels, each dissipating at least 1 mWatt of power into the structure. The detailed design of the gutter is primarily concerned with heat removal using axial air flow while maintaining structural rigidity.

The scope of this detector is well beyond that of devices presently being built by CDF and groups at CERN which contain $\sim 10^4$ channels. The CCD detector of SLD has large numbers of channels, but its readout is much too slow to be relevant for the hadron-collider environment.

As soon as the conceptual design allowed we started four projects to clarify the technical problems:

Figure 5: An end view of a BCD silicon vertex detector module. The preamplifier locations and strip orientation are indicated. The dashed lines refer to the ohmic side of the wafer and the solid lines refer to the diode side.

1. Mechanical construction: stability, alignment, heat dissipation, and cables.

   We consider the mechanical design the most challenging and difficult part of the vertex-detector R&D. Work on this critical topic has been undertaken at Fermilab by H. Jöstlein, C. Lindenmeyer, and coworkers.

2. The silicon detectors themselves: AC coupling, double sided readout.

   To help prepare for the effective use of new silicon detectors and readout chips, a program of evaluation of existing silicon strip detectors and chips has been carried out in the M-Test beam, headed by P. Karchin of Yale and P. Skubic of U. Oklahoma.

3. Electronics: specification of requirements, design and construction of a new chip (BVX).

   To reduce the mechanical complexities, the electronic readout design **must minimize both power dissipated and size and weight of the vertex-detector cable plant.** A VLSI design with substantial on-board digital processing can reduce the number of cables needed to read out the vertex detector.

   The 2.5-MHz crossing frequency of the Tevatron upgrade renders more difficult the task of designing low-noise preamplifiers with low power consumption. Further, there is

insufficient time between bunch crossing to have separate time frames for the operation of the analog and the digital circuitry. No existing readout chip combines these two functions with simultaneous operation.

We have embarked on an R&D program led by R. Yarema [10] of Fermilab to produce a new generation of readout chip, called the BVX chip. This chip could also be used in the readout of RICH counters, TRD's, or other devices not requiring a nsec timing capability, and will be the basis of a detector-wide integrated approach to the front-end electronics.

4. Detailed Monte Carlo simulation of the benchmark design.

   Simulations of the vertex detector system performance were begun by P. Karchin of Yale, L. Roberts of Fermilab (now SSCL), continued by K. McDonald of Princeton, and greatly extended by P. Lebrun of Fermilab.

2.1 Vertex-Detector Mechanical and Thermal Studies

The crucial requirement of the vertex-detector design is to **maintain the alignment to several microns over long times** within a module, once equilibrium temperature is reached. It was decided very early in the design stage that a mechanical/thermal model should be constructed. We describe the work over the last two years, led by H. Jöstlein of Fermilab. The majority of the work was done during the last two summers by two high-School science teachers, and by undergraduate students.

During the first year a full-scale brass model of the gutter was constructed, and alignment and cooling tests were performed. The following year we made improvements by adding dummy modules inside of the gutter to impede air flow. Sections 2.1.1-2.1.4 summarize this set of results. In parallel with the gutter tests, C. Lindenmeyer and H. Cease have been investigating the design and construction of the silicon modules, as discussed in Sec. 2.1.5. Section 2.1.6 outlines plans for future work at Fermilab (not to be funded by the SSC).

2.1.1 The Brass Gutter Model

The two halves of the support tube, called *gutters* because of the resemblance to rain troughs or gutters, were constructed of 10-mil-thick brass, since brass has approximately the same mechanical characteristics as beryllium. (The elastic modulus of brass is 16×10^6 lbs/in^2 while that of beryllium is higher, 42×10^6 lbs/in^2. The thermal expansion coefficients are 20.5×10^{-6}/°C and 11.3×10^{-6}/°C for brass and beryllium, respectively.) Webbings, also made of 10-mil brass, are soldered to the inside to add stiffness to the overall structure and to support the modules. Water channels are soldered to the outside of the gutter for cooling studies. The arrangement of the reinforcing webs is shown in Fig. 6.

The end view and support stand of the two halves of the gutter is shown in Fig. 7.

Eight heating strips were placed inside the gutter to simulate the 1-kW heat load from 1 million 1-mW preamplifiers. Cooling was accomplished with fans, blowing air in from the end of the gutter, and with water flowing in the brass channels on the surface of the gutter. The air- and water-cooling configuration is shown in Fig. 8.

Figure 6: The reinforcing-web arrangement shows the approximate spacing along the gutter and the holes that allow axial gas flow.

Figure 7: End view of the brass model of the gutter.

Figure 8: Air- and water-cooling configuration.

2.1.2 Mechanical and Thermal Study of the Gutter (1989)

The goal of the initial studies was to establish the stiffness and thermal stability of the two-gutter assembly, and the heat-removal capability of the cooling system [11]. Considerable effort was devoted to understanding the sources of experimental error in the measurements.

The gutter assembly was in the shape of a hexagonal prism, 120 inches long, and 9 inches in 'diameter.' The stiffness of the brass gutter assembly was such that is required an 800-gm weight applied at its midpoint to deflect the structure by 1 mil. The eventual Be gutter will have a modulus of elasticity, and hence stiffness, 2.5 times that of brass.

To study the thermal stability of the gutter it was cooled below ambient temperature by as much as 8°F and its position measured relative to a base at room temperature. Once the gutter was properly supported so that it was free to expand and contract, its motion was strictly consistent with the thermal-expansion coefficient of brass: 1 mil/°F over the 9-inch transverse width of the gutter. Recall that the thermal-expansion coefficient of brass is twice that of beryllium (and eight times that of silicon). Hence if we desire 5-μm mechanical stability, the beryllium-gutter temperature must be maintained constant to within 0.4°F.

In the third study, 1000 Watts of power were applied to the gutter via the heating strips. The consequent thermal expansion of the gutter was held to 1-2 mils by the combined cooling of 120 g/s air flow and 50 g/s water flow. Further studies showed that most of the cooling effect was due to the air flow and not the water; the heat transfer to the water needs to be improved. In this test no detector modules were mounted inside the gutter, and hence the impedance to the air flow was much less than will be the case in the full detector assembly.

2.1.3 Studies of Local Heating at the Amplifiers

The global heating studies of the gutter, described above, were followed by studies of the local heating of amplifiers on silicon detector modules [12]. Here the question was how hot would the amplifiers get under a nominal heat load, when cooled by an air flow. To answer this a model of a silicon detector module (Fig. 4) was constructed with resistors to simulate the local heat loads of the VLSI readout chips. Three such models were placed in the gutter and cooled with an air flow. During this study information was also obtained as to the

resistance of the detector modules to the air flow.

A complete module is expected to dissipate 150 Watts if each silicon strip channel consumes 1 mW. In the test, only 1/3 of one module was powered, to total load of 50 Watts. The air flow rate with the same fan as before, was now only 76 g/s, due to the air resistance of the three modules placed in the gutter. Temperature sensors were mounted on several of the powered resistors, and temperature rises of about 10°F were observed.

These results are encouraging in that if a nominal air flow of about 100 g/s can be delivered into the detector, the temperature rise at the amplifiers will be acceptably small – 10°F.

The air resistance per module was observed to be such that the pressure drop was 0.6 inches of water across the module. Hence a full detector of some 20 modules would require a pressure head of 12 inches of water = 0.03 atmospheres.

2.1.4 Further Tests (1990)

Additional tests were performed during 1990 [13]. They were studies of the thermal expansion of the gutter with 2000-Watts power dissipation, of the effects of mechanical impulses on the gutter, of vibration of the gutter with and without detector modules installed, and air-flow measurements with the detector modules in the gutter. Limits to the instrumentation were uncovered, in particular the large temperature sensitivity of the proximity sensors. Preliminary conclusions are:

- The proximity-sensor-readout electronics are sensitive to temperature. In some cases we found 30% of the apparent motion was due to temperature effects in the electronics. The instrumentation must be improved for further progress.
- The behavior of the gutter with 2000 Watts agrees in an understandable way with the results at 1000 Watts.
- There are known defects in the mechanical assembly of the first gutter that limit its utility in further studies.
- With brass mockups of the detector modules installed, there is significant vibration at the center of the gutter when the fan is on. Typical values are 0.03 mils peak-to-peak. However, the 3-point kinematical mount shields the module from the vibrations on the gutter. Typical values of vibration of the detector modules are less than 0.01 mils.
- With 3 detector modules installed, and 2000 Watts applied to the whole gutter assembly via heating strips, the air-temperature difference between the inlet and outlet of the gutter was found to be 45°F. This is much higher than desired, but is consistent with the reduced mass-flow rate (86 g/s) of the cooling air due to the resistance of the modules. It was not possible with the available fans to increase the mass-flow rate. When the needed flow-rate becomes available, we calculate that the resulting forces on the detector modules are still within acceptable limits; possible effects of vibrations must be explored.

2.1.5 Module Construction

The design for an individual silicon module is shown in Fig. 4. The silicon wafers themselves are the structural elements. These wafers are glued together with pyrex supports (manufactured by Newport Glass Works, Fig. 9) at the silicon-silicon joint for added strength with little additional material. The VLSI readout chips are glued directly to the silicon wafers. The R&D issues associated with the design are:

1. Mechanical rigidity of the glue joints.
2. Compatibility of the adhesive with electrical performance.
3. Local heating of the chips.
4. Cabling.
5. Accurate and feasible assembly techniques.

Figure 9: The pyrex prisms that support the silicon-silicon glue joint. **a)** the triangular prism for 90° joints. **b)** the chevron prism for 120° joints.

A evaluation of commercially available glues has been made by by H. Cease, an undergraduate student from IIT, and by C. Lindenmeyer of Fermilab. An acceptable adhesive must be strong, have good creep properties, be insensitive to radiation, and be soluble in some solution in case we need to dismantle the module for repair. Most importantly, the adhesive must not adversely affect the electrical performance of the silicon strip detectors.

Three adhesives were tested: Locktite 324 (a urethane methacrylate ester), NOA 81 (a UV-curing prepolymer acrylic), and Masterbond UV15-7 (a UV-curing epoxy). All three adhesives are soluable in trichloroethylene and methylene chloride.

A ‘T’-shape was formed with two pieces of silicon glued at right angles using the pyrex support at the joint, as shown in Fig. 10. A small weight was applied to the silicon and a proximity sensor was used to determine the deflection at various temperatures. All samples survived a 65-gram weight at 160°F for 3 hours without detectable motion. However, the NOA81 and Masterbond adhesives failed with an 85-gram weight after 30 minutes. All samples survived the 85-gram weight at 0°F for 3 hours.

Figure 10: The apparatus for tests of silicon-silicon glue joints. A test piece of silicon is glued at 90° to a vertical arm. A known force is applied to the end of the test piece, and its deflection monitored with an inductive position sensor.

In addition, ‘creep’ tests were performed over a period of a week and no creep was observed, although the silicon proved to be a good thermometer (see Fig. 11). Finally, we exposed the sample glue joints to a neutron flux of 10^{14} cm^{-2} at Argonne National Laboratory. No obvious ill effects were observed in any of the samples.

On the basis of these tests we concluded that the Locktite 324 adhesive is to be preferred.

One of the new DC-coupled multistripe Micron detectors (38×58 mm^2) was subjected to glueing tests. Locktite 324 adhesive was used to glue a 0.5-inch-long glass tube, and an SVX chip (bare silicon) onto the diode surface of this device. This particular device was chosen for a possibly destructive test as its ohmic side was inoperative. During curing, and subsequent cooling to -22°C, the operation of the device was monitored by observing the analog signal as displayed on an oscilloscope. Only minor glitches of the analog signal were observed; after full curing and cooldown over a few hours, the operation of the device returned completely to normal. Subsequently the device was suspended in a bath of methylene chloride for 12 hours to dissolve the Locktite 324 and release the glass tube and SVX chip. After this, the operation of the device was again normal. Additionally, H. Cease glued and unglued other pieces of silicon and glass onto the ohmic side; and examination under a microscope showed no discernable damage.

We consider these results to be very encouraging, allowing us to proceed with confidence to glueing of detectors into a self-supporting structure, with readout chips glued directly to

Figure 11: Results of the 'creep' test of the Locktite 324 adhesive over one week. While no net displacement was observed, the joint expanded and contracted in proportion to the ambient temperature.

the detectors.

We are now ready to study the effect of local heating of the silicon detector by the readout preamplifier. The increased heating tends to decrease the signal/noise performance of the readout chip and may cause the glue to soften. It may also affect the performance of the readout chip itself. Increased cooling or an alternate method of mounting the readout chips may be necessary.

An (uninstrumented) silicon module has been assembled in Spring 1991 by hand by H. Cease, and rather convincingly demonstrates the viability of an all-silicon structure. This assembly used the pyrex support prisms and the Locktite 324 adhesive. In the near future this model will undergo cooling and mechanical tests.

On another front, C. Lindenmeyer has been studying possible assembly procedures for the modules that will not be excessively labor intensive and that can attain the required accuracy [14]. He has developed assembly plans using special fixtures and a 3-axis coordinate-measuring machine. Once the lessons from the hand assembly of the first module have been assimilated, further progress will require access to such a machine.

2.1.6 Future Gutter and Module Studies

The building and testing of this model has been labor intensive; large amounts of data have been recorded and analysed. The construction and study of this model has been very instructive. However, this model has been pushed to its limits. A new model is necessary,

built to more exacting specifications. The proximity sensors are now being replaced by ones with greater accuracy; the old set was limited to about 0.5-mil accuracy, while a new set constructed by D. Chissus (1991 High-School Teacher Summer Intern at Fermilab) has achieved < 1-μm accuracy. The gutter must be redesigned and constructed of beryllium since the brass flexes during heating and cooling. A suspension-type support structure of the gutter assembly is needed if we are to advance beyond the problems associated with mounting it directly on a steel table. The air-flow system is inadequate and needs at minimum a new pump. The liquid-cooling system was not optimized and more channels, perhaps of different shapes, should be used on a new model. In addition, the model will have to be located in an environmentally controlled room as our results indicate we are sensitive to temperature shifts.

The next step would be a system test of a full-length gutter loaded with all the silicon modules, of which a number of wafers would be instrumented. Besides the usual mechanical and thermal studies, the assembly would be placed in the test beam and the performance studied.

Finally, our understanding of many of the issues has progressed to the point where we would like to initiate a simulation of the model to proceed in parallel with the laboratory studies. This simulation should use a finite-element analysis program such as ANSYS, and should incorporate both a stress-analysis and heat-flow study.

The work described in this subsection is to be performed by Fermilab personnel [15].

2.2 The BVX Readout Chip

The initial work on readout issues generated the specifications for the BVX chip, taking into account the broader issues of the B-physics goals and overall approach to triggering. It has taken a year to fine-tune the specifications of the BVX chip, and some topics are still not completely resolved. For example, a fast out that provided trigger information was considered too difficult at this early stage, but is something that we will undoubtedly wish to consider later since a vertex trigger would be extremely useful to a B-physics experiment.

The R&D program has begun to test hardware solutions to subsets of the full specifications via so-called tiny chips, submitted to the MOSIS VLSI-chip facility. A short summary of this work is presented following a list of the BVX specifications.

2.2.1 BVX Specifications

We list the technical specifications of the BVX for the interested reader. No attempt is made to put them in the context of existing chips, but in general the parameters are slightly beyond those achieved in existing chips while being within reach of new efforts, especially as silicon technologies with smaller feature sizes become available. A simplified BVX block diagram is given in Fig. 12.

1. Detectors will be double-sided AC coupled. For a switched-capacitor circuit this implies double-correlated sampling to correct for integrator charge-injection effects, offsets, and input-drift effects. Circuitry must be designed for positive and negative signals.

Figure 12: A block diagram of the BVX readout chip. There are 3 stages: amplification, storage, and digitization/sparsification. Digitization takes place only after a Level-1 trigger accept.

2. 128 channels/chip including an amplifier and digital section that run simultaneously (in contrast to the separate data-acquisition and data-readout cycles of the SVX chip).
3. Digitized signal and address outputs.
4. On-board A/D conversion with 7 bit accuracy and a conversion time of 1-2 μs.
5. A direct analog output for diagnostic purposes.
6. Input-amplifier total response and reset time of 400 ns, corresponding to a 2.5-MHz interaction rate.
7. Input-amplifier noise = 600 $e_{\rm rms}$ at $C_{\rm in}$ = 5 pf. This is determined by a 200-μm-thick fully depleted silicon detector and a signal of 5000 electrons per strip from a 55°-angle-of-incidence track.
8. On-board 16-bucket analog memory for each of 128 channels. This gives 6.4 μs of delay to allow for the Level-1 trigger-decision time.
9. 4-bit Level-1-trigger FIFO to store information after the Level-1-trigger accept. This allows for simultaneous data-readout and data-acquisition cycles and provides time for

the on-board digitization. Data reduction from analog memory to the FIFO is about 50:1.

10. An event number via a 4-bit counter that gets bumped with each Level-1 accept.
11. Events are not necessarily read out in order. They will be assembled downstream of the BVX.
12. One discriminator per channel, with a common threshold for 128 channels and one calibration input for the 128 channels.
13. Data sparsification of the digital outputs, with the option of reading all channels for debugging.
14. Must be able to daisy chain analog and digital outputs from up to 10 chips.
15. Option to suppress the readout of a chip if there are more than 10-20 hits on the chip. We expect typically 1-2 hits/chip per event.
16. Option to gate off unwanted channels.
17. Design for 1-2 mW power consumption per channel.
18. The chip should withstand about 100 krads/year of radiation.
19. Assume the input capacitance is a maximum of about 5pf and the amplifier pitch is less than 50μm.

2.2.2 Summary of Progress

The BVX readout R&D effort encompasses four topics: preamplifier design, A/D design, the study of simultaneous analog and digital operation, and radiation hardness.

Preamplifier Design

The amplifier design has been done in collaboration with C. Britton of ORNL. Two devices have been designed, fabricated and tested. One was a preamplifier (called IIA) and one was a preamplifier/shaper. There is a new preamplifier designed and presently in layout, and a new preamplifier/shaper in layout, both due to be submitted in November. The MOSIS facility was used and the test chips were fabricated in a 2-μm CMOS process.

A real-time-feedback amplifier design, similar to the CERN AMPLEX, was chosen for IIA. This design contrasts with the switched-capacitor technique used in the SVX chip. A circuit diagram of the IIA preamp/shaper is given in Fig. 13.

Three input-transistor W/L designs were studied: 1000/2, 1500/2, and 2000/2, all on a 45-μm pitch, with channel lengths 4700 μm, 4830 μm, and 5060 μm, respectively. The shaper lengths were all the same, namely 2014 μm. The calculated and measured performance of preamplifier IIA with a total shaping time of 450 ns are listed in Table 1. The shaper was external to the circuit and the noise is shown for two input capacitances.

Figure 13: The BVX IIA test preamplifier and shaper circuit.

Table 1: Noise performance of the BVX IIA preamp.

Input	Noise Equivalent	
Capacitance	Calculated	Measured
5 pf	301 e	510 e
16.5 pf	582 e	910 e

These numbers are very encouraging for the first design pass and indicate that the noise goals are probably achievable. The estimated power dissipation for the IIA preamplifier and shaper is 1.2 mW.

The IIIA design has only a slight change to the preamp, but we added a second stage to the shaping to provide higher gain for the A/D. The main problem at this point is a ±2-fC DC offset at the shaper output which can lead to higher noise. This problem is being studied. Another problem is the physical size of the chip, which will be reduced somewhat with a smaller-feature-size process, but most of that reduction comes from the digital section. In

addition, as is well known by the experts, fabrication of a high-value feedback resistor is difficult.

As a comparison, the SVX-H preamplifier, fabricated in a 1.2-μm radiation-soft process, was tested. The preamp is of the switched-capacitor type, the input W/L was 500/3 μm, and it operated with a gain of 26 mV/fC. In the double-correlated-sampling mode, and with a partial reset (which we do not describe), the noise figures are presented in Table 2.

Table 2: Noise performance of the SVX-H preamp.

Input Capacitance	Noise (e)	Shaping Time (ns)
5 pf	700	340
10 pf	1000	360
30 pf	2000	480

A full reset (if the integrator needs resetting) gives about the same noise figures but roughly doubles the shaping times. For reference, the present SVX-D (quad-correlated sampling) with 30-pf input capacitance has a noise figure of 2100 electrons.

We are considering a mixed-mode approach, where the first stage of the preamplifier contains a feedback resistor, and subsequent stages of shaping use the switched-capacitor approach. This may solve the DC-offset problem of the feedback-preamp design mentioned earlier.

A/D Converter

It became clear early in our considerations that a single A/D per channel would be necessary if high data rates were to be achieved. We have designed, laid out, and submitted for fabrication an 8-channel Wilkinson ADC. The device has 7-bit accuracy, with the 8th bit being used for data sparsification. It has been laid out on a 45-μm pitch using 2-μm technology. Eventually a 1.2-μm feature size will be used, and the chip will run faster and be smaller in size. A block diagram of the ADC is presented in Fig. 14.

The expected power consumption is 300 μW. The conversion time for 7-bit accuracy is 2.56 μs, (full-scale σ) using a 25-MHz clock. The readout time is very fast, typically 240 ns for 8 channels. The test chip is expected within a couple of weeks.

Simultaneous Analog and Digital Operation

A test stand to explore simultaneous analog and digital operation has been built. The bonding wires have been shown to cause significant coupling from output to input. An output-to-input capacitance (stray capacitance) of 0.1 ff causes a 0.5-fC input for a 5-volt logic swing.

Figure 14: A block diagram of the Wilkinson ADC and data readout.

A test chip was built that included an isolation barrier. The chip contains two ring counters and preamplifier. The amplifier output was studied and the evidence of noise is shown in Fig. 15 as well as the effect of the isolation. Study of this problem is continuing.

Radiation Hardness

A nondisclosure agreement with UTMC for fabricating radiation-hard devices has been made by Fermilab. The design rules are in-house for the 1.2-μm process. This work is just beginning and we expect to collaborate with other high-energy-physics institutions that are also just starting to work with UTMC.

2.3 Bench Tests of Silicon Strip Detectors

Charge-correlation measurements of several DC-coupled microstripe detectors have been made at U. Oklahoma [16, 17]. The tests were made with a Sr^{90} source, with the detectors operated at $-22°$C. The correlation of the charges collected from both the diode ("holes") and the ohmic ("electrons") stripes are equal within a signal-to-noise resolution of 30:1 (*i.e.*, 800 electrons noise) using common-mode-subtracted double-correlated sampling with a 300-ns integrating time via the Berkeley SVXD readout chip.

The detectors were double-sided DC coupled devices manufactured by Micron Semiconductor, Ltd. (Sussex, England). Each device was made from a 3″ silicon wafer and had overall dimensions 38 mm $\times$ 58 mm $\times$ 300 μm thickness, although, for these tests only a fraction of the available area (the same for each device) was instrumented for readout. Both sides of each device were divided into three regions according to pitch (see Fig. 16) – a central

Figure 15: Scope display of noise pickup in simultaneous analog/digital operation. The ring counter can be seen as noise at the preamplifier output. The isolation eliminates this problem.

region of 25-μm pitch was surrounded on each side by a region of 50-μm pitch. This division was effected so that the variation of performance characteristics with pitch (charge sharing, resolution, *etc.*) could be studied conveniently on a single device.

Stripes on each of the diode and ohmic sides of each detector were read out with the Berkeley SVXD IC [22]. These chips were mounted on fan-in cards with a 50-μm pitch to receive wirebonded detector channels. Two SVX chips were used to read out each side.

The readout of the SVX chips was accomplished with a Berkeley microprogrammable SVX readout Sequencer ("SRS") and fast ADC ("SDA") modules [23] which were built and

Figure 16: The geometric layout of the Micron Si-strip detector, showing three regions of differing stripe pitch.

tested at Oklahoma. A block diagram of the readout electronics is shown in Fig. 17.

A principal result of the study was the demonstration of a systematic correlation between the ohmic- and diode-side pulse heights for the same events with the same detector. (Such a correlation would be expected since the ionizing particle produces both electrons, which migrate to the ohmic side, and an equal number of holes, which migrate to the diode side of the device.) In Figure 18b we show a scatter plot of diode- *vs.* ohmic-side pulse heights for a sample of events from the 50-μm-pitch region of the detector, when exposed to a Sr^{90} source. The signal is taken as the largest sum of three adjacent pulse heights, since the charge is typically deposited in more than one stripe. On the plot, a perfect correlation with no noise spread and equal "gains" would show up as a straight line with a 45° slope. It is seen that there is a strong correlation between ohmic- and diode-side pulse heights.

Figures 18a and 18d show the ohmic- and diode-side pulse-height histograms as projected from the scatter plot of Fig. 18b. The rms noise width can be determined from the difference between the signals on the ohmic and diode sides, as shown in Fig. 18c. The observed σ of 6

Figure 17: Block diagram of the Si-strip readout electronics.

counts is $\sqrt{2}$ times the rms noise on each side separately, which is therefore about 4 counts. Thus the signal-to-noise is about 18 to 1 on each side in this study.

Continuations of these studies with improved control over the electronics have now shown signal-to-noise of 30:1.

2.4 Beam Tests of Silicon Strip Detectors

We have recently completed the first portion of a test program on silicon microstrip detectors with VLSI readout in the M-Test beam. In 1990 we operated single- and doubled-sided AC-coupled detectors from two manufacturers, SI (Oslo) and MBB (Munich), while in 1991 we studied the double-sided DC-coupled detectors from Micron that were described in Sec. 2.3. All detectors were instrumented with the Berkeley SVX version D silicon-strip-readout chip. These chips were interfaced using the Berkeley SRS fast-sequencer and SDA flash-ADC modules. Measurements were made of the signal-to-noise and spatial resolution for tracks at normal and non-normal angle of incidence [18, 19].

Figure 18: Evidence for charge correlation between signals on the ohmic and diode sides of a DC-coupled Si-strip detector. **a)** the diode-side pulse heights; **b)** the ohmic- *vs.* diode-side signals; **c)** the difference between the ohmic- and diode-side signals; **d)** the ohmic-side signal.

The silicon strip detectors were mounted in the fixture sketched in Fig. 19, which could orient them at various angles to the beam. Three of the four detectors would be used to define a particle track, so the resolution of the fourth detector could be determined as a function of angle of incidence. The results are shown in Fig. 20, for measurements on the side of a Micron detector for which the stripes are perpendicular to the plane of incidence, so an inclined track deposits charges over several stripes. The rms noise per stripe was only 800-1000 electrons, which permits the relatively slow deterioration of resolution with increasing angle of incidence.

Figure 19: The mounting fixture for silicon-strip-detectors in the M-Test beam-line. Three of the detectors could be rotated so the beam was at non-normal incidence.

Figure 20: The measured spatial resolution in a double-sided DC-coupled Si-strip detector (Micron) as a function of the angle of incidence. The detector stripes are perpendicular to the plane of incidence.

2.5 Simulation of Vertex-Detector Performance

Monte Carlo simulations of the BCD vertex detector were begun by P. Karchin and L. Roberts [20], continued by K. McDonald [2], and extended by P. Lebrun [21]. We summarize here some of the advances of the latter work, which is still in progress.

In the recent simulations a full analysis program for tracking and vertexing in the silicon detector has been written. It is presented with fake data from a Monte Carlo simulation in the form of ADC counts in and addresses of struck detector elements. This very considerable effort is perhaps unique in that the BCD has its primary analysis program written before the experiment is approved!

Features of the simulation are listed below. Advances over previous work are noted.

1. Events containing B-$\overline{B}$ jets are generated using ISAJET and transmitted to GEANT for detector simulation. Multiple-scattering effects are included in the track propagation. The simulation includes a uniform, transverse magnetic field of 10 kG, as specified for the full BCD experiment. This is the first of our simulations to include a magnetic field.

2. The model silicon detector, sketched in Figs. 3-5, contains some 1.2×10^6 silicon strips.

3. Figure 21 shows the multiplicity distributions of all particles, charged particles, and number of struck strips in the vertex detector for the simulated events.

4. The response of each silicon detector to passing charged particles is modelled, including Landau fluctuations in the deposited energy, charge sharing among adjacent strips, and noise in the readout amplifiers. The signal (plus noise) charge is analyzed in a 7-bit ADC, and the ADC counts in each silicon detector channel are written to tape, simulating a raw-data file.

5. Track pattern recognition is performed using a hypothesis as to a track road as would be provided in an outer straw-tube tracking system. Simulated noise counts, and multiple tracks crossing a single detector strip lead to confusion in the pattern recognition, as illustrated in Fig. 22.

6. The raw strip pulse heights are searched for clusters, corresponding to single-particle tracks. A hit must be above a pulse-height threshold before it is included in the cluster analysis. In a 4π-solid-angle geometry many particles cross the silicon detectors at large angles of incidence, leading to large clusters as sketched in Fig. 23. The summed ADC counts over strips in clusters in disk detectors is shown in Fig. 24.

7. The hit clusters on different silicon detectors are then searched for tracks. Roads are taken from an assumption of track finding in an outer tracking detector not simulated here. In the presence of a nonzero magnetic field the track roads are helical. Figure 25 shows the multiplicity distribution of hit clusters used on the reconstructed tracks.

8. When two hit clusters in a silicon detector are within 3σ of one another in one coordinate, where σ is the r.m.s. cluster width, they are said to be confused.

Figure 21: Multiplicity distributions for **a)**: all particles, **b)**: charged particles, and **c)**: struck silicon strips in the simulated events.

Figure 26 shows the confusion probability as a function of strip length for barrel detectors. If the confusion probability is desired to be at most 1%, the strips must be no longer than 1 cm, which leads to a large channel count for the whole detector.

9. Once the tracks have been found, and the errors on the fitted trajectories evaluated, vertex finding is begun. The primary vertex is found first, and tracks with poor fits to this vertex are searched for secondary vertices. The invariant-mass distribution of the tracks to secondary vertices can then be examined for B-meson decays, *etc.*

   All algorithms needed for this have been written and appear to be working. However, the results are too preliminary to justify making firm conclusions about the detector performance at this time.

Figure 22: Confusion due to multiple hits in a silicon detector arises when two tracks pass through the same, or closely adjacent, strips.

Figure 23: Hit clusters from tracks in a silicon detector. Tracks with large angles of incidence lead to extensive clusters with small pulse height in each strip.

Figure 24: The pulse-height spectrum for hit clusters in silicon disk detectors.

Figure 25: Multiplicity of hits per reconstructed track in the silicon vertex detector.

From these studies we will soon have rather realistic estimates of track and vertex finding in the silicon vertex detector in the presence of electronic noise and signals from large numbers of tracks. From this one can extrapolate the signal-to-background ratio in measurements of various B-decay modes, estimate the accuracy on proper-time measurements, *etc.* A question of importance for the μBCD (and also to upgrades of CDF and D0) is how well does the silicon vertex detector perform as a standalone tracker?

Figure 26: Hit-confusion probability in the barrel detectors as a function of silicon strip length.

3 Proposed Continuation of the R&D Program

To demonstrate the feasibility of a silicon vertex detector with interleaved disks and barrels we propose to build two 'inner-hexagon' modules of instrumented detectors, as sketched in Fig. 27. These modules could then be tested in a fixed-target beamline with a target on the axis of the detector to provide multiple tracks at angles representative of those to be encountered in a collider experiment.

The inner-hexagon module is comprised of three types of silicon detectors, which we will call A, B, and C, as shown in Fig. 28. Type A forms the inner barrel, Type B forms the disks, and Type C forms the outer barrel. To have good acceptance of tracks near 45° angle there should be two disks per module. The Type B detectors are not actually arrayed in planes, but in a stepped pattern that permits a spiral path for cooling-air flow through the detector. An indication of the offsets of the six Type B detectors per module is shown in the side view of Fig. 27. There are a total of six Type A, six Type B, and six Type C detectors in each inner-hexagon module.

Although it is not part of the present proposal, eventually we would like to build the larger modules shown previously in Figs. 3-5. Such modules have three barrel layers, and require two additional detector types, shown in Fig. 29. Two Type E detectors lie along each face of the outer hexagonal prism, as a single full-length detector could not be made out of a 4″ wafer. It requires a total of 42 detectors to build one large hexagonal module.

We now discuss the various steps needed to bring the inner-hexagon modules into existence.

3.1 Design of the Type A, B, and C Detectors

DC-coupled detectors of the size and shape of Type C have already been fabricated for us by Micron Semiconductor, and tested as described in Secs. 2.3 and 2.4. Production of AC-coupled Type C detectors is well underway, and a first fabrication run was made in Summer 1991. The second run, now in progress, incorporates an improvement to the metallization of

Figure 27: End and side views of an inner-hexagon module.

Figure 28: Type A, B, and C silicon detectors, shown relative to a $4''$ silicon wafer.

Figure 29: Type D, and E silicon detectors, shown relative to a 4″ silicon wafer. Extra Type A detectors could be incorporated on the Type E wafer to provide test detectors.

the 'foxFET' gate which controls the reverse-bias current. While two Type C detectors can fit on a 4″ wafer, a single one can fit on a 3″ wafer, which we plan to use in this case only.

The Type A and B detectors can be placed on a single 4″ wafer to save on the cost of the mask sets. The design for the Type A, and B detectors will begin in early 1992, with first production in Spring 1992. A large order for a total of 54 Type A, B, and C detectors (18 each) could be placed at the beginning of FY93. This would provide enough detectors for three modules, assuming no damage in construction, or more practically, two complete inner-hexagon modules.

3.2 SVX Chip Carriers

Each inner-hexagon module requires 240 128-channel SVX chips to be completely instrumented. There are thus 30,720 channels per inner-hexagon module.

While the SVX chips are now readily available, we must develop a suitable carrier for these chips. The carrier will be glued to a silicon detector, and a row of SVX chips glued to the carrier. The carrier serves to distribute the DC power to the row of chips, and to provide a bus of digital-control and analog-output lines. A custom cable is attached to one end of each chip carrier to connect the chips to the external readout and power circuitry. The chip carrier can also serves as a heat sink to decrease thermal gradients in the SVX chips.

Chip carriers of much of the desired functionality have been developed by CDF for their barrel vertex detector [24]. However, these are physically larger than are suitable for mounting directly on the Type A, B, and C detectors. Also, it would be advantageous to make the chip carriers from aluminum nitride, rather than alumina, because of the superior thermal

conductivity of the former. For this we propose to undertake a development program with Promex (Santa Clara).

3.3 Custom Cabling

To bring power and control onto the SVX chips, and the data off them, we need to develop a set of flexible low-mass cable, each having 16 130-Ω pairs of signal lines and 4 DC-power strips. These ($\sim$ 30-cm-long) cables must be quite flexible to reach the SVX chip on the inside surfaces of the inner-hexagon module.

These cables run to a PC board close to the inner-hexagon modules, that includes a bidirectional switch for the I/O control lines, and passes the data signals on to a conventional cable for transmission to the CAMAC readout modules.

3.4 Readout

For a demonstration of the feasibility of the inner-hexagon module we need a readout system for up to 60,000 channels, but this need not be high speed. For this the CAMAC-based SVX readout system [23] is sufficient, if used in sparse-readout mode. We propose to purchase two new sets of these (one SRS and two SDA's each), one set for each of the two inner-hexagon modules.

3.5 Mechanical and Thermal Modelling

The techniques for assembly of an instrumented inner-hexagon module must be demonstrated. While the basic viability of a self-supporting silicon structure has been shown by us, as discussed in Sec. 2.1.5, new assembly fixtures must be made that accommodate detectors with chip, carriers and cables already attached.

A cooling system for the 2-mWatt/channel = 60 Watt/module heat load must also be demonstrated. While we believe that a forced-'air' (N_2 or Ar) cooling system will suffice (see Secs. 2.1.2-2.1.4), this remains to be proven for a module with the extra impedance of the chip carriers and cables. Should the forced-air system prove to be inadequate we would explore the refrigerant systems under development at Los Alamos [25].

To begin work on these issues, we will use a simplified module, consisting of four Type C detectors glued together to form an open rectangular box.

The mechanical accuracy of the assembly can be verified by a coordinate-measuring machine recently purchased at Princeton U. The machine may also be used in some steps of assembly to insure precision alignment of the detectors [14].

3.6 System Test

The proposed R&D will culminate in a system test in a fixed-target beam.

The inner-hexagon modules permit a 3-cm-diameter beam pipe to be inserted along the axis of the modules. A solid target placed inside of the pair of modules in a low-energy test beam would yield several particles per interaction through the detectors. Off line, the signals from several events could be superimposed to simulate very high multiplicity events.

This test should be adequate to demonstrate the viability of a silicon vertex detector with interleaved disks and barrels.

4 Budget Proposal for FY92

The R&D program proposed in Sec. 3 is a two-year program. The budget presented below is the total projected for the two years. Ideally, equal funding would be available in each of the two years, as the costs for development in the first year are similar to those for production in the second year.

4.1 University of Oklahoma

In FY92 we will finalize our design of doubled-sided AC-coupled silicon detectors with Micron Semiconductor, and evaluate the initial production run. We will also develop aluminum-nitride carrier boards, and special cabling from the SVX chips to the readout modules. In FY93 we will complete the production of 54 Type A,B, and C detectors, and attach them, together with the aluminum-nitride carriers to the inner-hexagon modules, which will then be tested in a fixed-target beamline.

1. Permanent Equipment

1. 5 double-sided AC-coupled Si-strip detectors (Type C) $15k
2. Masks for Types A and B Si-strip detectors $20k
3. Production run of 54 Type A, B, and C Si-strip detectors $100k
4. SVX chips $5k
5. Development of aluminum-nitride carriers $20k
6. Production run of 54 aluminum-nitride carriers $10k
7. Development of custom readout cabling $20k
8. MAC-IIci computer, CAMAC crate and interface $10k
9. CAMAC SVX readout modules $15k
10. NIM crate, hex discri, quad coincidence, gate generator scaler $10k
11. Waveform generator (Wavetek 20-MHz) $3k
12. Spectrum analyzer (Tek 2712 or HP 8591A) $10k
13. Digital oscilloscope (Tek TDS540) $12k

Total Permanent Equipment $250k

2. Materials, Supplies, and Travel

1. Assembly fixtures $5k

2. Glues, solvents $1k
3. UV lamp $1k
4. Miscellaneous supplies $10k
5. Travel $8k

Total Materials, Supplies, and Travel $25k

Indirect Costs of 46% on Materials, Supplies, and Travel $12k

3. Total University of Oklahoma $287k

4.2 Princeton University

In FY92 we will construct mechanical and thermal models of a prototype vertex detector module consisting of only four detectors. In FY93 we will construct and test the inner-hexagon modules with Type A, B, and C detectors developed by U. Oklahoma.

1. Permanent Equipment

1. 5 double-sided AC-coupled Si strip detectors (Type C) $15k
2. Cooling system $20k
3. PC-clone computer, CAMAC crate and interface $10k
4. CAMAC SVX readout modules $15k
5. Temperature sensors (Keithley 7057A) $3k
6. Readout scanner (Keithley 706) $2k
7. x-y translation stage, stepper motor control $5k
8. NIM crate, hex discri, quad coincidence, gate generator scaler $10k

Total Permanent Equipment $80k

2. Materials, Supplies, and Travel

1. Test-grade silicon wafers $2k
2. Glass prisms $5k
3. Laser cutting of test wafers $2k
4. Assembly fixtures $5k
5. Glues, solvents $1k
6. UV lamp $1k
7. Miscellaneous supplies $12k
8. Travel $5k

Total Materials, Supplies, and Travel **$33k**

Indirect Costs of 67% on Materials, Supplies, and Travel **$22k**

3. Total Princeton University **$135k**

5 Personnel

5.1 Langston University

A recent collaboration has begun between Langston U. and U. Oklahoma under the auspices of the Prairie View Detector Center funded by the Texas National Research Laboratory Commission. D. Gunter and I. Husein and undergraduate students will participate in this project. Initial work will concentrate on testing silicon detectors and readout circuits under the direction of G. Kalbfleisch of U. Oklahoma. This initiative will constitute the first steps in bringing Langston U. into the high-energy-physics-research community.

5.2 University of Oklahoma

In FY92 a new graduate student, T. Vaughn, will join the O.U. silicon effort. Additional graduate students are expected to join in mid 1992 as J. Kuehler and M. Wood move on to their Ph.D thesis projects. A new Postdoctoral Research Associate will be hired in FY92 using funds from the TNRLC. Assistant Prof. P. Gutierrez will continue to be partially involved. This R&D project will continue to be a major component of Prof. G.R. Kalbfleisch's research program.

5.3 Princeton University

J.G. Heinrich and C. Lu will work full time on R&D for SSC subsystems. K.T. McDonald will spend 90% of his research time in these projects. Graduate students W.S. Anderson, and one other to be named shortly will devote all their research effort to this project. In addition, we benefit from access (at no cost to the SSC) to the technical staff of the Princeton High Energy Physics group which includes 1 mechanical engineers, 3 mechanical technicians, 1 electrical engineer, and 3 electrical technician. All salaries of the above people are supported by the DoE HEP Division, except for K.T. McDonald (academic year salary from Princeton University), and W.S. Anderson (NSF Predoctoral Fellow).

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