Progress Report and Renewal Request for R&D on

A Silicon Vertex Detector with Interleaved Disks and Barrels

(Submitted to the Superconducting Super Collider Laboratory)

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Summary

For a B-physics experiment at a hadron collider, the large angular range of the B-decay products leads to the requirement of a silicon vertex detector with interleaved disk and barrel detectors. As no present or approved collider experiment uses this geometry we have undertaken an R&D program to demonstrate its viability. We report on progress on mechanical modelling, development of custom VLSI readout chips, bench and beam tests of silicon detectors, and on simulations of system performance. We propose a two-year continuation of this program to produce two hexagonal modules of fully instrumented silicon detectors. For this we seek a budget of **$287k** at U. Oklahoma and **$135k** at Princeton U., with 50% of the funding in each of FY92 and FY93.

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1 Introduction

A B-physics experiment at the SSC would be an excellent extension of the Higgs-sector program already underway via SDC and GEM. We have presented a preliminary vision of such an experiment in EOI0008 [1, 2].

The critical component of a B-physics detector is the silicon vertex detector. For an experiment at the SSC collider the vertex detector should cover a large rapidity range to maximize the acceptance of the low-transverse-momentum B's. Present collider detectors (CDF, MarkII, ALEPH, DELPHI, OPAL) all have vertex detectors with a 'barrel' configuration matched to the central rapidity region. Fixed-target experiments all have planar detector configurations. The best option for a collider B-physics experiment is, we believe, a configuration of interleaved 'barrels' and planar 'disks' of silicon detectors. We expand on this view in Sec. 1.1 below.

No presently approved experiment anywhere plans to use such a configuration. Hence if the community is to be convinced of its viability, a demonstration must be made as a new R&D effort. The BCD collaboration has been engaged in first steps in such an R&D program since 1989 [3, 4, 5, 6, 7], but the results are not yet definitive. Here we propose a program to complete the demonstration of a prototype barrel and disk module in two years, so as to influence in a timely manner the possible inauguration of a B-physics program at the SSC.

1.1 The Need for Interleaved Barrels and Disks

The silicon vertex detector must locate the secondary vertex of the B's ($c\tau \approx 360$ μm) to isolate the B-decay products from the high-multiplicity primary event. The broad range of angles of the B-decay products leads to the need for a complicated configuration of the vertex detector. If we only desired to observe tracks at small angles to the beams we would use an array of 'disks' as sketched in Fig. 1a, while for large angles a 'barrel' array (Fig. 1b) would be ideal. However, we cannot build a large-solid-angle vertex detector out of separate disk and barrel modules for two reasons:

1. The finite length of the luminous region blurs the correlation between a silicon detector's position and its angle from the primary vertex, as shown in Fig. 2. Hence the barrel detectors must extend over a length roughly that of the luminous region.

2. The vertex resolution of both disk and barrel detectors is determined by the radius at which the first measurement is made, as discussed in the following paragraph. (This result contrasts with the use of the detectors for momentum measurement, where the total path length observed is the critical parameter.) Hence the disk detectors cannot be backed off to make room for the enlarged barrel detector without sacrificing vertex resolution.

   We illustrate the claim in the preceding paragraph with a simplified calculation of vertex resolution. Suppose the vertex detector consists of only two disks, at z_1 and z_2. From measurements of coordinates r_1 and r_2 we extrapolate a straight-line fit back to $z = 0$ and use $r(0)$ as the measure of fit to the primary vertex. Each of

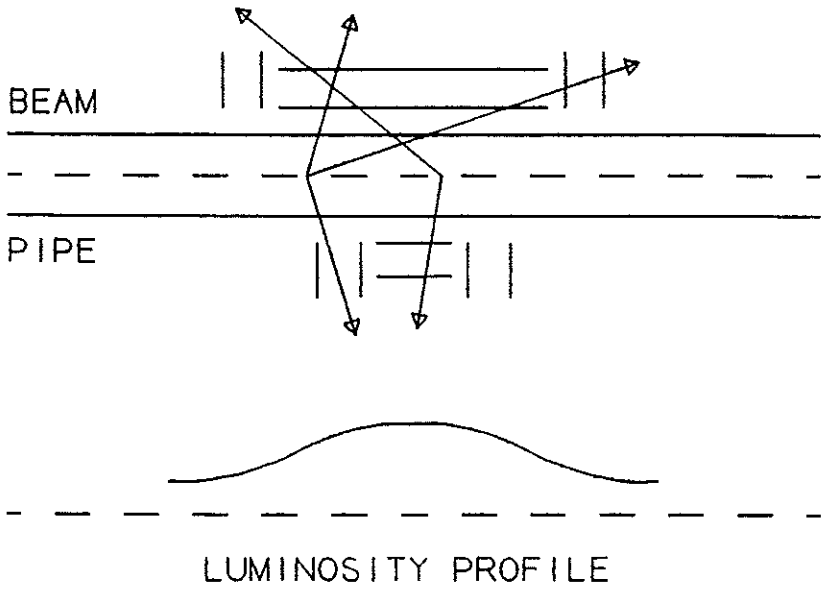

Figure 2: A vertex detector with separate disk and barrel silicon does not give optimal angular coverage if the luminous region has a finite extent.

in the extrapolated value $z(0)$ has the same form as that just found for $\sigma_{r(0)}$ but with the $\cos^{3/2}\theta$ changed to $\sin^{3/2}\theta$. Hence both disk and barrel detectors must begin at very small radii.

We conclude that it is vital to build a vertex detector with interpenetrating regions of disks and barrels if both large- and small-angle tracks are to be analyzed.

2 Progress Report

Besides the authors of the present document, our R&D program involves collaborators from Fermilab, IIT, and ORNL. In this Section we review all facets of our silicon detector R&D. The specific proposal for new work to be supported by the SSC Subsystem R&D Program is given in Sec. 3.

The silicon vertex detector for a hadron collider is, by necessity, ambitious and complex. The basic design criteria have already been discussed in the introduction. Considerations of full acceptance (roughly ± 4 units of pseudorapidity), low mass, and the finite size of the interaction region lead to a device 3-4 m long, 10-20 cm in radius, and containing 1-2 square meters of double-sided AC-coupled silicon detectors. A spatial accuracy of 5-7 μm for angles of incidence up to 60° on the detector requires detectors of strip pitch 25-50 μm and digitization of the signals, which can only be accomplished in a cost-effective manner with on-detector VLSI chips with ambitious specifications. This detector will have in excess of 1 million channels distributed over $\sim$ 1000 wafers.

There have been several iterations of the vertex detector concept, starting with a design which placed the silicon detectors inside of the vacuum pipe, which was largely the work of P.

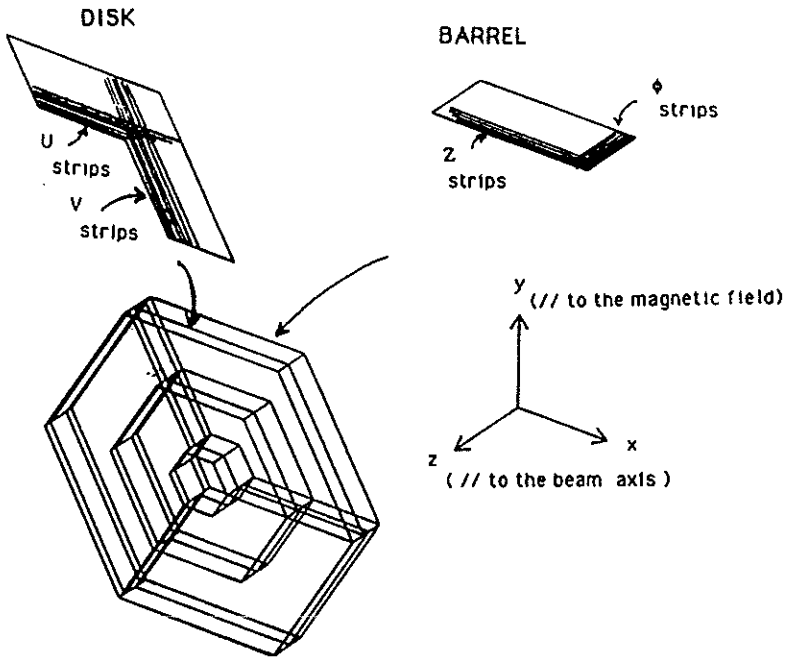

Figure 4: A representation of a single module of the Central portion of the vertex detector shown in Fig. 3. Disk and barrel silicon detectors are glued together into a hexagonal structure. The disks are mounted in a helicoidal pattern to allow a net longitudinal air flow through the detector for cooling. The stripes on the disk detectors are aligned along u and v axes which permits the readout chips to be placed at the outer edges only. The inner radius of the silicon is 1.5 cm, and the outer is 10 cm. Each module is 4.8 cm long.

therefore simplify the design. One consequence of the long design is that an equally long support structure is needed. This structure must bear the load of all the modules and yet be composed of a thin, low-Z material to minimize multiple-scattering effects. The proposed structure is a beryllium cylindrical tube, 10-20 cm in radius and is called a **gutter**.

3. The vertex detector will contain more than 1 million readout channels, each dissipating at least 1 mWatt of power into the structure. The detailed design of the gutter is primarily concerned with heat removal using axial air flow while maintaining structural rigidity.

The scope of this detector is well beyond that of devices presently being built by CDF and groups at CERN which contain $\sim 10^4$ channels. The CCD detector of SLD has large numbers of channels, but its readout is much too slow to be relevant for the hadron-collider environment.

As soon as the conceptual design allowed we started four projects to clarify the technical problems:

insufficient time between bunch crossing to have separate time frames for the operation of the analog and the digital circuitry. No existing readout chip combines these two functions with simultaneous operation.

We have embarked on an R&D program led by R. Yarema [10] of Fermilab to produce a new generation of readout chip, called the BVX chip. This chip could also be used in the readout of RICH counters, TRD's, or other devices not requiring a nsec timing capability, and will be the basis of a detector-wide integrated approach to the front-end electronics.

4. Detailed Monte Carlo simulation of the benchmark design.

   Simulations of the vertex detector system performance were begun by P. Karchin of Yale, L. Roberts of Fermilab (now SSCL), continued by K. McDonald of Princeton, and greatly extended by P. Lebrun of Fermilab.

2.1 Vertex-Detector Mechanical and Thermal Studies

The crucial requirement of the vertex-detector design is to **maintain the alignment to several microns over long times** within a module, once equilibrium temperature is reached. It was decided very early in the design stage that a mechanical/thermal model should be constructed. We describe the work over the last two years, led by H. Jöstlein of Fermilab. The majority of the work was done during the last two summers by two high-School science teachers, and by undergraduate students.

During the first year a full-scale brass model of the gutter was constructed, and alignment and cooling tests were performed. The following year we made improvements by adding dummy modules inside of the gutter to impede air flow. Sections 2.1.1-2.1.4 summarize this set of results. In parallel with the gutter tests, C. Lindenmeyer and H. Cease have been investigating the design and construction of the silicon modules, as discussed in Sec. 2.1.5. Section 2.1.6 outlines plans for future work at Fermilab (not to be funded by the SSC).

2.1.1 The Brass Gutter Model

The two halves of the support tube, called *gutters* because of the resemblance to rain troughs or gutters, were constructed of 10-mil-thick brass, since brass has approximately the same mechanical characteristics as beryllium. (The elastic modulus of brass is 16×10^6 lbs/in^2 while that of beryllium is higher, 42×10^6 lbs/in^2. The thermal expansion coefficients are 20.5×10^{-6}/°C and 11.3×10^{-6}/°C for brass and beryllium, respectively.) Webbings, also made of 10-mil brass, are soldered to the inside to add stiffness to the overall structure and to support the modules. Water channels are soldered to the outside of the gutter for cooling studies. The arrangement of the reinforcing webs is shown in Fig. 6.

The end view and support stand of the two halves of the gutter is shown in Fig. 7.

Eight heating strips were placed inside the gutter to simulate the 1-kW heat load from 1 million 1-mW preamplifiers. Cooling was accomplished with fans, blowing air in from the end of the gutter, and with water flowing in the brass channels on the surface of the gutter. The air- and water-cooling configuration is shown in Fig. 8.

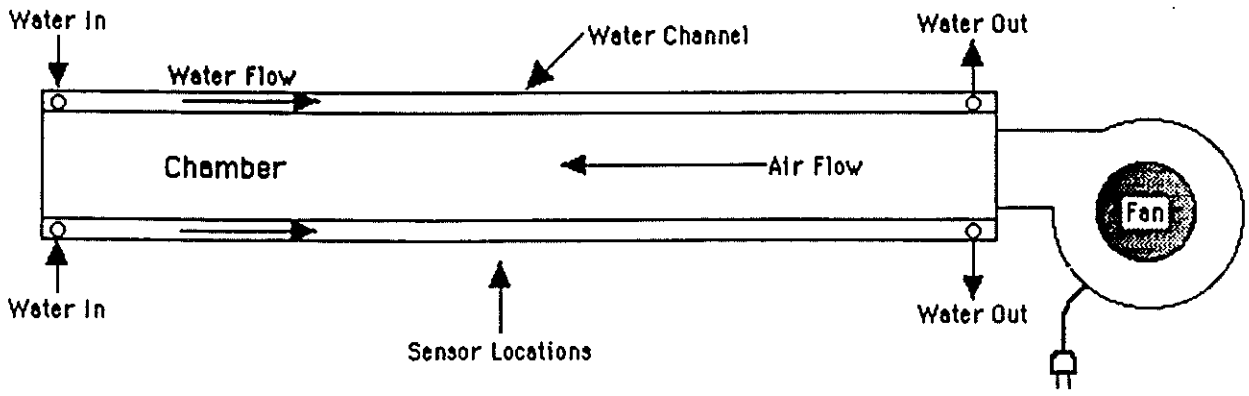

Figure 8: Air- and water-cooling configuration.

2.1.2 Mechanical and Thermal Study of the Gutter (1989)

The goal of the initial studies was to establish the stiffness and thermal stability of the two-gutter assembly, and the heat-removal capability of the cooling system [11]. Considerable effort was devoted to understanding the sources of experimental error in the measurements.

The gutter assembly was in the shape of a hexagonal prism, 120 inches long, and 9 inches in 'diameter.' The stiffness of the brass gutter assembly was such that is required an 800-gm weight applied at its midpoint to deflect the structure by 1 mil. The eventual Be gutter will have a modulus of elasticity, and hence stiffness, 2.5 times that of brass.

To study the thermal stability of the gutter it was cooled below ambient temperature by as much as 8°F and its position measured relative to a base at room temperature. Once the gutter was properly supported so that it was free to expand and contract, its motion was strictly consistent with the thermal-expansion coefficient of brass: 1 mil/°F over the 9-inch transverse width of the gutter. Recall that the thermal-expansion coefficient of brass is twice that of beryllium (and eight times that of silicon). Hence if we desire 5-μm mechanical stability, the beryllium-gutter temperature must be maintained constant to within 0.4°F.

In the third study, 1000 Watts of power were applied to the gutter via the heating strips. The consequent thermal expansion of the gutter was held to 1-2 mils by the combined cooling of 120 g/s air flow and 50 g/s water flow. Further studies showed that most of the cooling effect was due to the air flow and not the water; the heat transfer to the water needs to be improved. In this test no detector modules were mounted inside the gutter, and hence the impedance to the air flow was much less than will be the case in the full detector assembly.

2.1.3 Studies of Local Heating at the Amplifiers

The global heating studies of the gutter, described above, were followed by studies of the local heating of amplifiers on silicon detector modules [12]. Here the question was how hot would the amplifiers get under a nominal heat load, when cooled by an air flow. To answer this a model of a silicon detector module (Fig. 4) was constructed with resistors to simulate the local heat loads of the VLSI readout chips. Three such models were placed in the gutter and cooled with an air flow. During this study information was also obtained as to the

2.1.5 Module Construction

The design for an individual silicon module is shown in Fig. 4. The silicon wafers themselves are the structural elements. These wafers are glued together with pyrex supports (manufactured by Newport Glass Works, Fig. 9) at the silicon-silicon joint for added strength with little additional material. The VLSI readout chips are glued directly to the silicon wafers. The R&D issues associated with the design are:

1. Mechanical rigidity of the glue joints.
2. Compatibility of the adhesive with electrical performance.
3. Local heating of the chips.
4. Cabling.
5. Accurate and feasible assembly techniques.

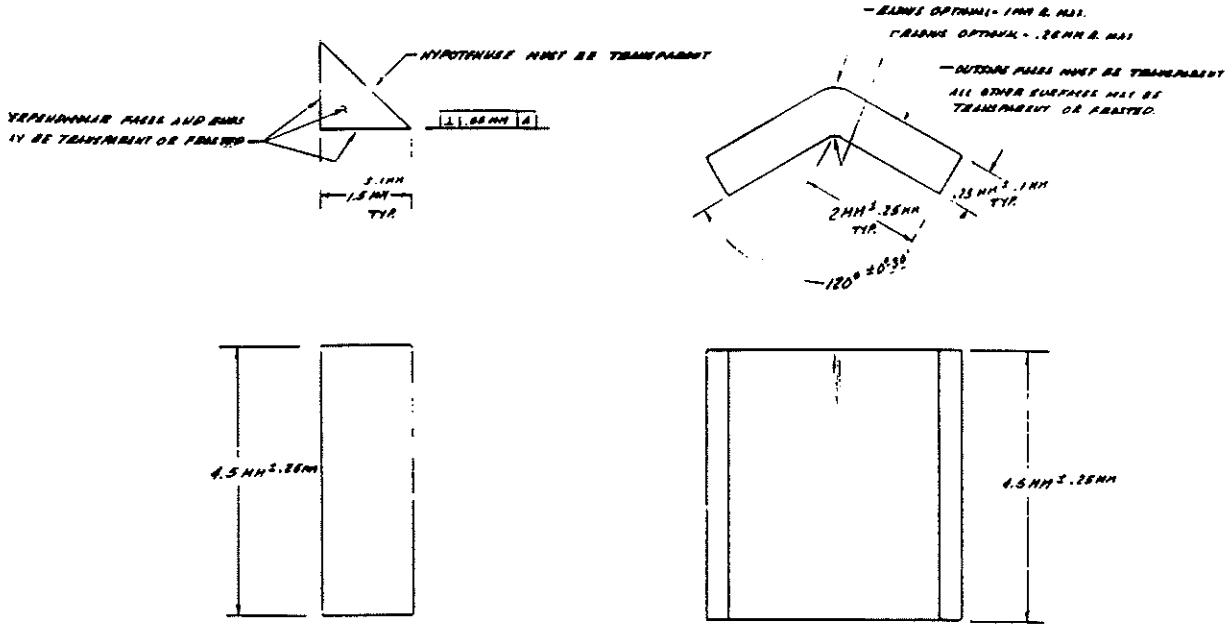

Figure 9: The pyrex prisms that support the silicon-silicon glue joint. a) the triangular prism for 90° joints. b) the chevron prism for 120° joints.

A evaluation of commercially available glues has been made by by H. Cease, an undergraduate student from IIT, and by C. Lindenmeyer of Fermilab. An acceptable adhesive must be strong, have good creep properties, be insensitive to radiation, and be soluble in some solution in case we need to dismantle the module for repair. Most importantly, the adhesive must not adversely affect the electrical performance of the silicon strip detectors.

Three adhesives were tested: Locktite 324 (a urethane methacrylate ester), NOA 81 (a UV-curing prepolymer acrylic), and Masterbond UV15-7 (a UV-curing epoxy). All three adhesives are soluable in trichloroethylene and methylene chloride.

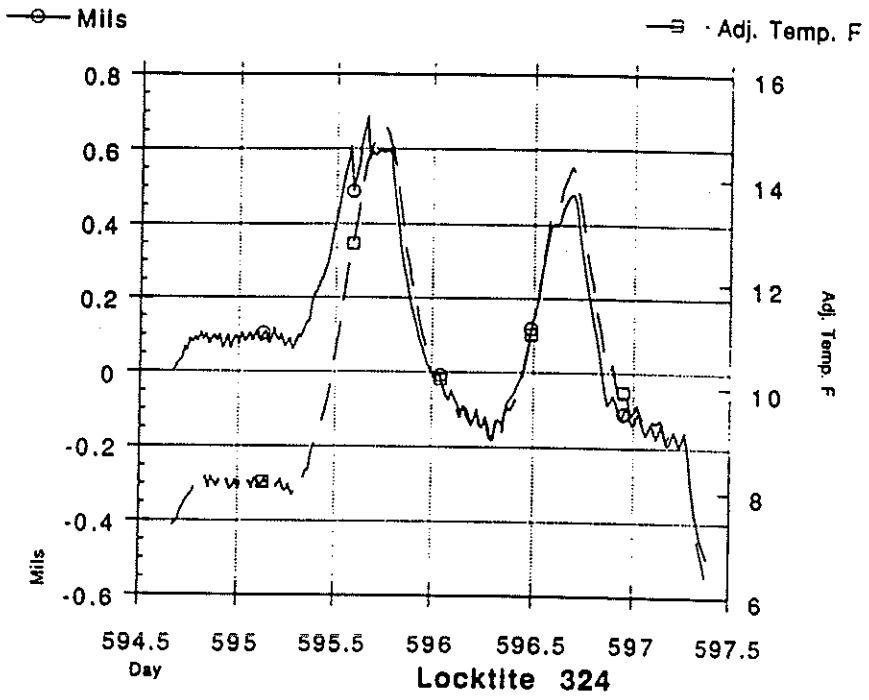

Figure 11: Results of the 'creep' test of the Locktite 324 adhesive over one week. While no net displacement was observed, the joint expanded and contracted in proportion to the ambient temperature.

the detectors.

We are now ready to study the effect of local heating of the silicon detector by the readout preamplifier. The increased heating tends to decrease the signal/noise performance of the readout chip and may cause the glue to soften. It may also affect the performance of the readout chip itself. Increased cooling or an alternate method of mounting the readout chips may be necessary.

An (uninstrumented) silicon module has been assembled in Spring 1991 by hand by H. Cease, and rather convincingly demonstrates the viability of an all-silicon structure. This assembly used the pyrex support prisms and the Locktite 324 adhesive. In the near future this model will undergo cooling and mechanical tests.

On another front, C. Lindenmeyer has been studying possible assembly procedures for the modules that will not be excessively labor intensive and that can attain the required accuracy [14]. He has developed assembly plans using special fixtures and a 3-axis coordinate-measuring machine. Once the lessons from the hand assembly of the first module have been assimilated, further progress will require access to such a machine.

2.1.6 Future Gutter and Module Studies

The building and testing of this model has been labor intensive; large amounts of data have been recorded and analysed. The construction and study of this model has been very instructive. However, this model has been pushed to its limits. A new model is necessary,

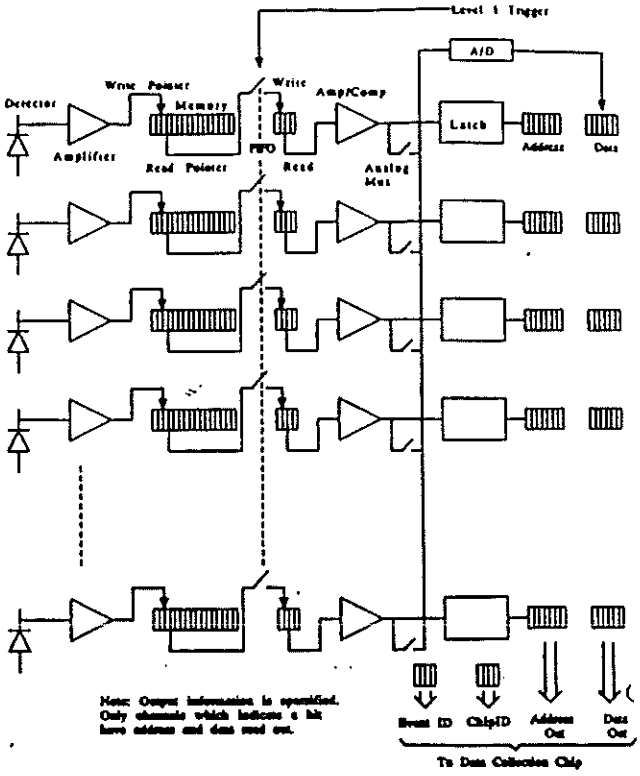

Figure 12: A block diagram of the BVX readout chip. There are 3 stages: amplification, storage, and digitization/sparsification. Digitization takes place only after a Level-1 trigger accept.

2. 128 channels/chip including an amplifier and digital section that run simultaneously (in contrast to the separate data-acquisition and data-readout cycles of the SVX chip).

3. Digitized signal and address outputs.

4. On-board A/D conversion with 7 bit accuracy and a conversion time of 1-2 μs.

5. A direct analog output for diagnostic purposes.

6. Input-amplifier total response and reset time of 400 ns, corresponding to a 2.5-MHz interaction rate.

7. Input-amplifier noise = 600 $e_{\rm rms}$ at $C_{\rm in}$ = 5 pf. This is determined by a 200-μm-thick fully depleted silicon detector and a signal of 5000 electrons per strip from a 55°-angle-of-incidence track.

8. On-board 16-bucket analog memory for each of 128 channels. This gives 6.4 μs of delay to allow for the Level-1 trigger-decision time.

9. 4-bit Level-1-trigger FIFO to store information after the Level-1-trigger accept. This allows for simultaneous data-readout and data-acquisition cycles and provides time for

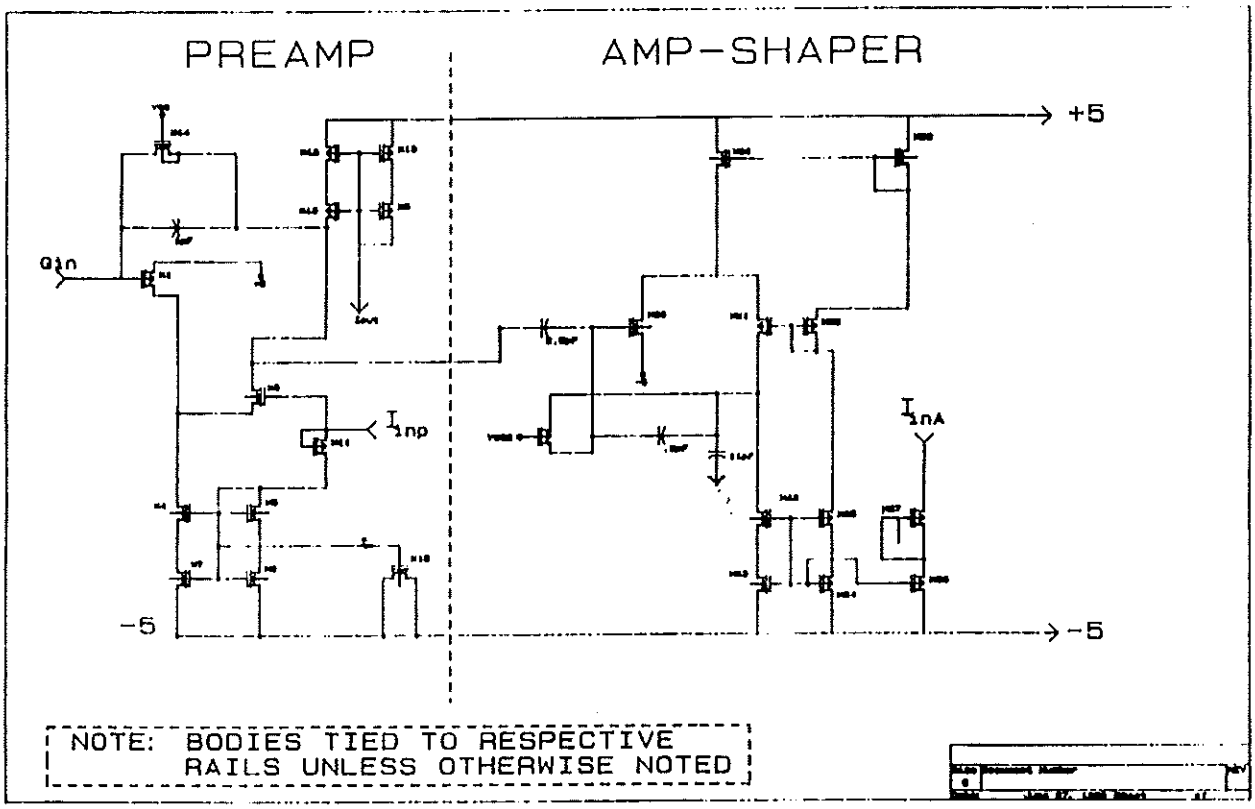

Figure 13: The BVX IIA test preamplifier and shaper circuit.

Table 1: Noise performance of the BVX IIA preamp.

Input	Noise Equivalent	
Capacitance	Calculated	Measured
5 pf	301 e	510 e
16.5 pf	582 e	910 e

These numbers are very encouraging for the first design pass and indicate that the noise goals are probably achievable. The estimated power dissipation for the IIA preamplifier and shaper is 1.2 mW.

The IIIA design has only a slight change to the preamp, but we added a second stage to the shaping to provide higher gain for the A/D. The main problem at this point is a $\pm$2-fC DC offset at the shaper output which can lead to higher noise. This problem is being studied. Another problem is the physical size of the chip, which will be reduced somewhat with a smaller-feature-size process, but most of that reduction comes from the digital section. In addition, as is well known by the experts, fabrication of a high-value feedback resistor is difficult.

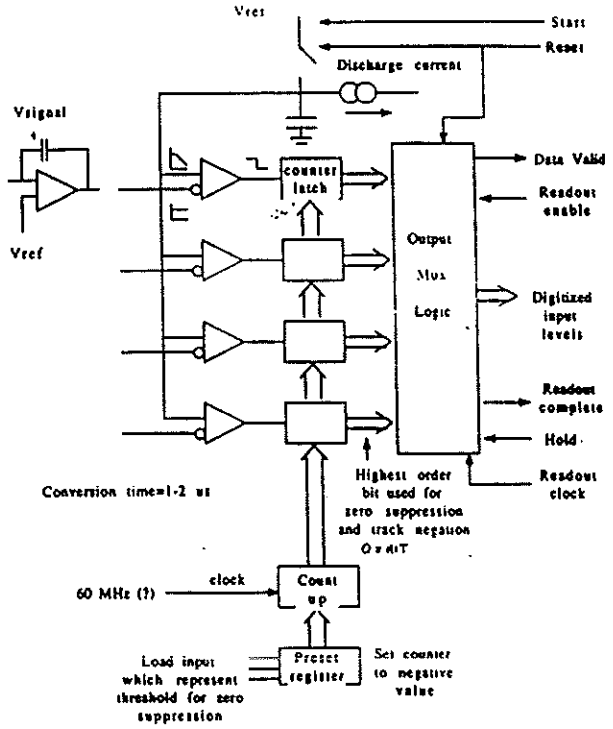

Figure 14: A block diagram of the Wilkinson ADC and data readout.

A nondisclosure agreement with UTMC for fabricating radiation-hard devices has been made by Fermilab. The design rules are in-house for the 1.2-μm process. This work is just beginning and we expect to collaborate with other high-energy-physics institutions that are also just starting to work with UTMC.

2.3 Bench Tests of Silicon Strip Detectors

Charge-correlation measurements of several DC-coupled microstripe detectors have been made at U. Oklahoma [16, 17]. The tests were made with a Sr^{90} source, with the detectors operated at $-22°C$. The correlation of the charges collected from both the diode ("holes") and the ohmic ("electrons") stripes are equal within a signal-to-noise resolution of 30:1 (*i.e.*, 800 electrons noise) using common-mode-subtracted double-correlated sampling with a 300-ns integrating time via the Berkeley SVXD readout chip.

The detectors were double-sided DC coupled devices manufactured by Micron Semiconductor, Ltd. (Sussex, England). Each device was made from a 3″ silicon wafer and had overall dimensions 38 mm × 58 mm × 300 μm thickness, although, for these tests only a fraction of the available area (the same for each device) was instrumented for readout. Both sides of each device were divided into three regions according to pitch (see Fig. 16) – a central region of 25-μm pitch was surrounded on each side by a region of 50-μm pitch. This division was effected so that the variation of performance characteristics with pitch (charge sharing, resolution, *etc.*) could be studied conveniently on a single device.

Stripes on each of the diode and ohmic sides of each detector were read out with the Berkeley SVXD IC [22]. These chips were mounted on fan-in cards with a 50-μm pitch to

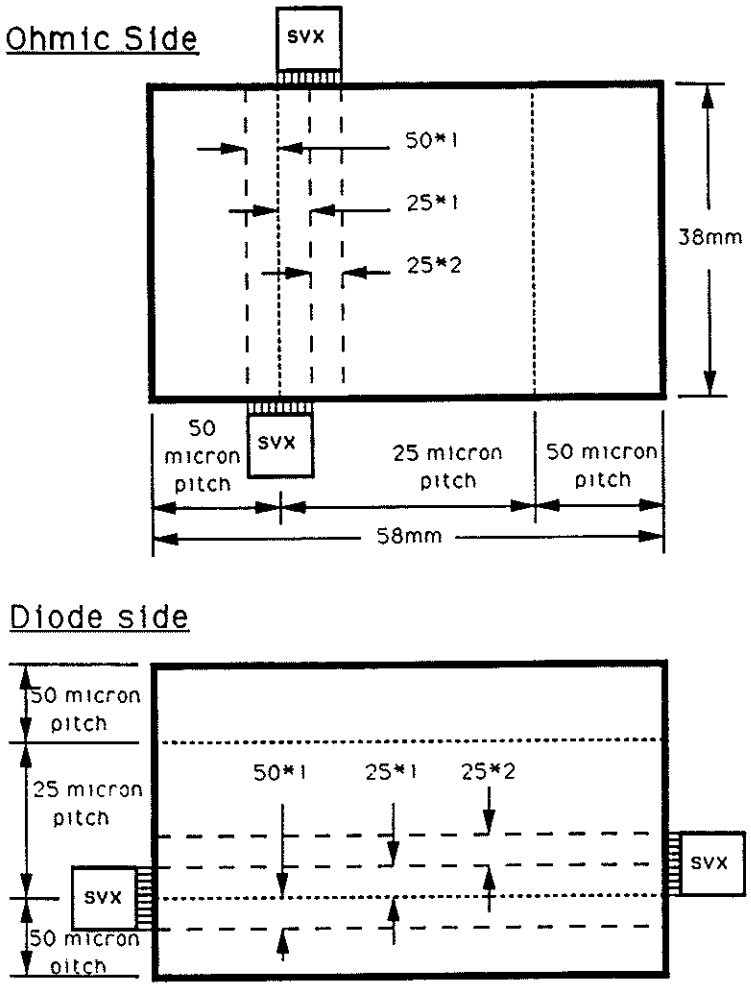

Figure 16: The geometric layout of the Micron Si-strip detector, showing three regions of differing stripe pitch.

the device.) In Figure 18b we show a scatter plot of diode- *vs.* ohmic-side pulse heights for a sample of events from the 50-μm-pitch region of the detector, when exposed to a Sr^{90} source. The signal is taken as the largest sum of three adjacent pulse heights, since the charge is typically deposited in more than one stripe. On the plot, a perfect correlation with no noise spread and equal "gains" would show up as a straight line with a 45° slope. It is seen that there is a strong correlation between ohmic- and diode-side pulse heights.

Figures 18a and 18d show the ohmic- and diode-side pulse-height histograms as projected from the scatter plot of Fig. 18b. The rms noise width can be determined from the difference between the signals on the ohmic and diode sides, as shown in Fig. 18c. The observed σ of 6 counts is $\sqrt{2}$ times the rms noise on each side separately, which is therefore about 4 counts. Thus the signal-to-noise is about 18 to 1 on each side in this study.

Continuations of these studies with improved control over the electronics have now shown signal-to-noise of 30:1.

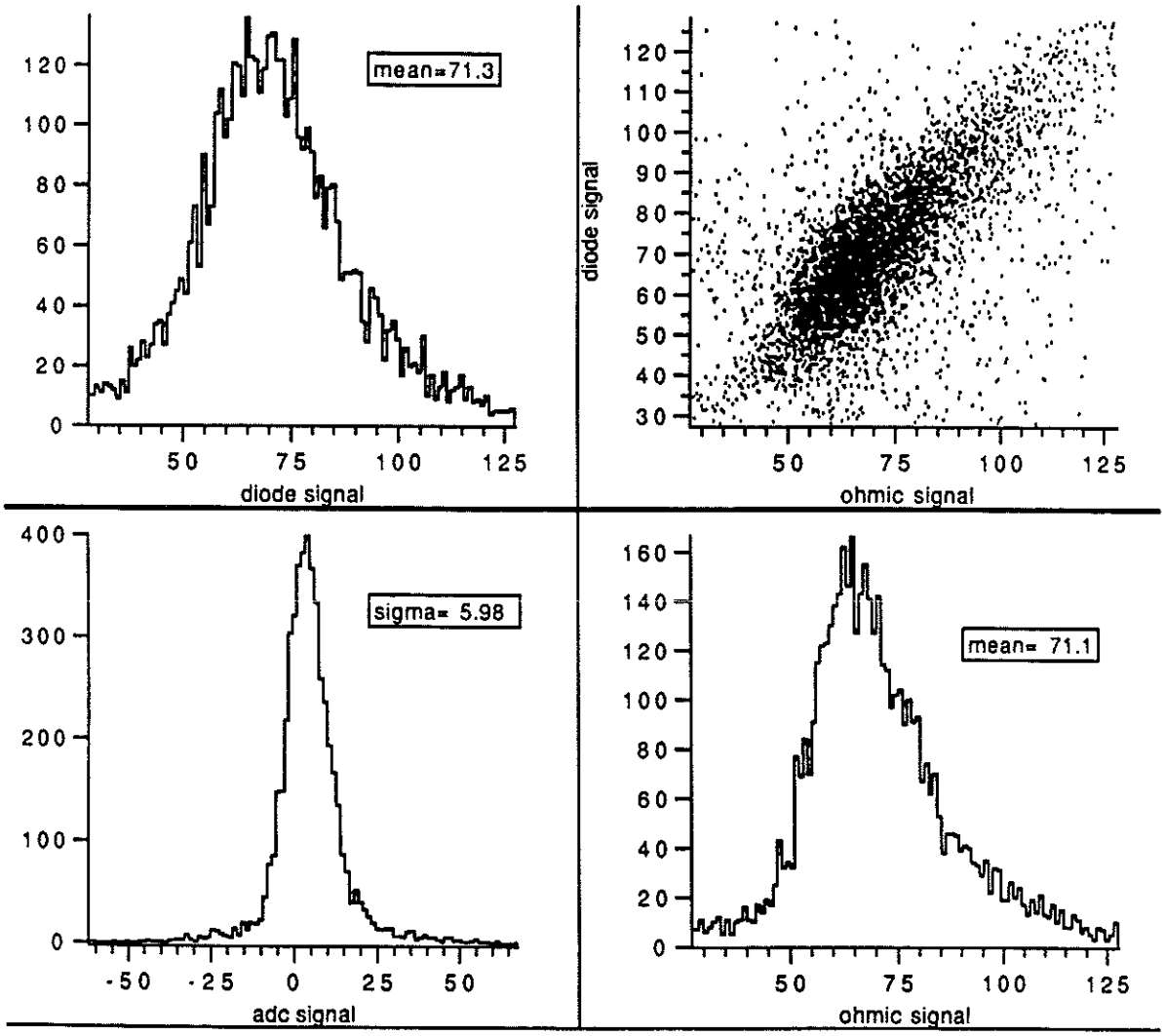

Figure 18: Evidence for charge correlation between signals on the ohmic and diode sides of a DC-coupled Si-strip detector. a) the diode-side pulse heights; b) the ohmic- *vs.* diode-side signals; c) the difference between the ohmic- and diode-side signals; d) the ohmic-side signal.

only 800-1000 electrons, which permits the relatively slow deterioration of resolution with increasing angle of incidence.

2.5 Simulation of Vertex-Detector Performance

Monte Carlo simulations of the BCD vertex detector were begun by P. Karchin and L. Roberts [20], continued by K. McDonald [2], and extended by P. Lebrun [21]. We summarize here some of the advances of the latter work, which is still in progress.

In the recent simulations a full analysis program for tracking and vertexing in the silicon detector has been written. It is presented with fake data from a Monte Carlo simulation in

the form of ADC counts in and addresses of struck detector elements. This very considerable effort is perhaps unique in that the BCD has its primary analysis program written before the experiment is approved!

Features of the simulation are listed below. Advances over previous work are noted.

1. Events containing B-$\bar{B}$ jets are generated using ISAJET and transmitted to GEANT for detector simulation. Multiple-scattering effects are included in the track propagation. The simulation includes a uniform, transverse magnetic field of 10 kG, as specified for the full BCD experiment. This is the first of our simulations to include a magnetic field.

2. The model silicon detector, sketched in Figs. 3-5, contains some 1.2×10^6 silicon strips.

3. Figure 21 shows the multiplicity distributions of all particles, charged particles, and number of struck strips in the vertex detector for the simulated events.

4. The response of each silicon detector to passing charged particles is modelled, including Landau fluctuations in the deposited energy, charge sharing among adjacent strips, and noise in the readout amplifiers. The signal (plus noise) charge is analyzed in a 7-bit ADC, and the ADC counts in each silicon detector channel are written to tape, simulating a raw-data file.

5. Track pattern recognition is performed using a hypothesis as to a track road as would be provided in an outer straw-tube tracking system. Simulated noise counts, and multiple tracks crossing a single detector strip lead to confusion in the pattern recognition, as illustrated in Fig. 22.

6. The raw strip pulse heights are searched for clusters, corresponding to single-particle tracks. A hit must be above a pulse-height threshold before it is included in the cluster analysis. In a 4π-solid-angle geometry many particles cross the silicon detectors at large angles of incidence, leading to large clusters as sketched in Fig. 23. The summed ADC counts over strips in clusters in disk detectors is shown in Fig. 24.

7. The hit clusters on different silicon detectors are then searched for tracks. Roads are taken from an assumption of track finding in an outer tracking detector not simulated here. In the presence of a nonzero magnetic field the track roads are helical. Figure 25 shows the multiplicity distribution of hit clusters used on the reconstructed tracks.

8. When two hit clusters in a silicon detector are within 3σ of one another in one coordinate, where σ is the r.m.s. cluster width, they are said to be confused.

   Figure 26 shows the confusion probability as a function of strip length for barrel detectors. If the confusion probability is desired to be at most 1%, the strips must be no longer than 1 cm, which leads to a large channel count for the whole detector.

9. Once the tracks have been found, and the errors on the fitted trajectories evaluated, vertex finding is begun. The primary vertex is found first, and tracks with poor fits to this vertex are searched for secondary vertices. The invariant-mass distribution of the tracks to secondary vertices can then be examined for B-meson decays, *etc.*

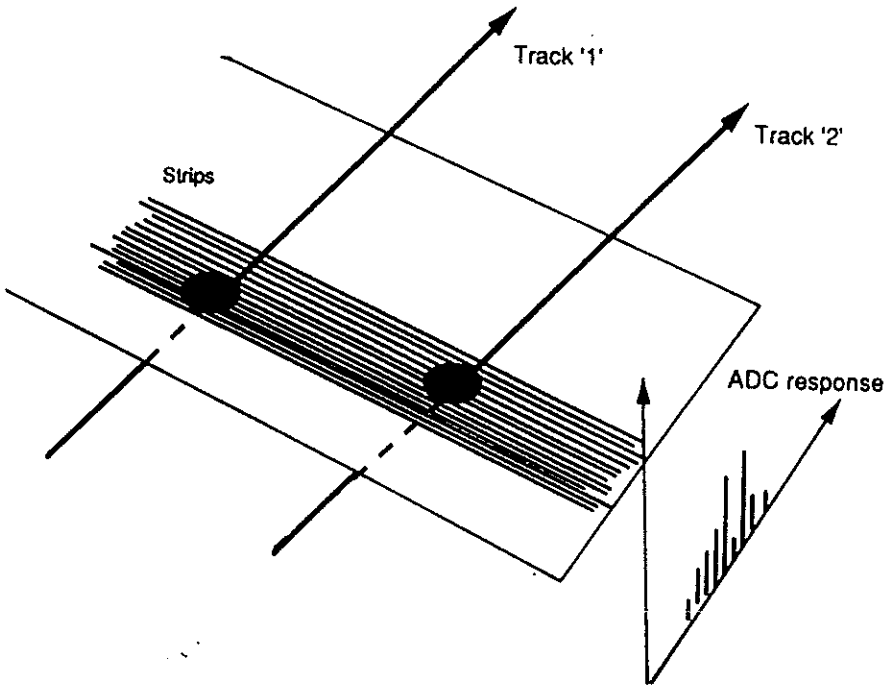

Figure 22: Confusion due to multiple hits in a silicon detector arises when two tracks pass through the same, or closely adjacent, strips.

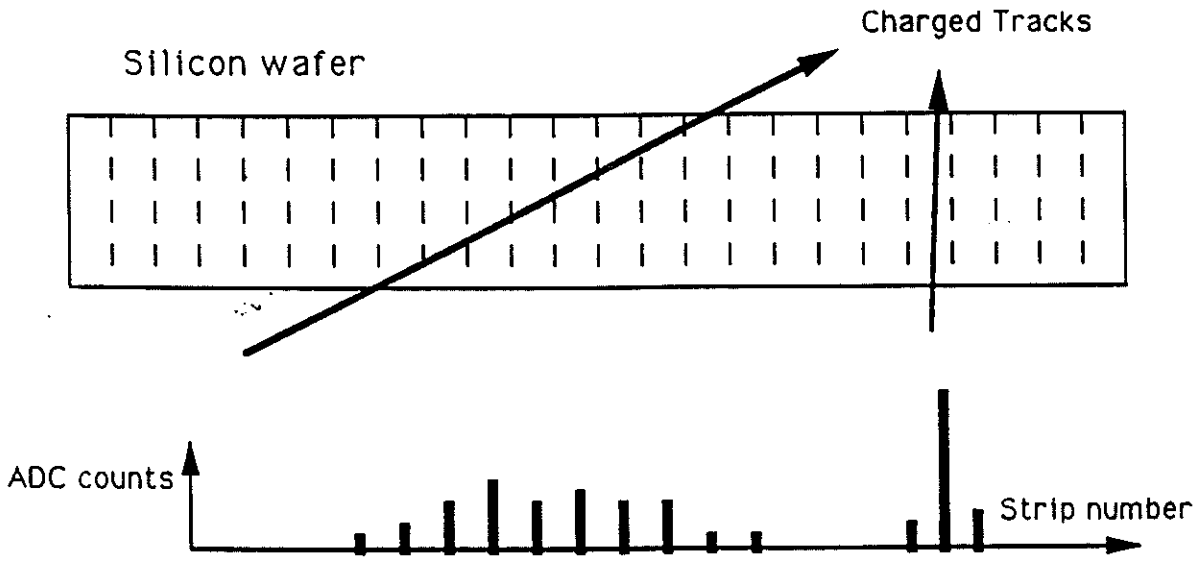

Figure 23: Hit clusters from tracks in a silicon detector. Tracks with large angles of incidence lead to extensive clusters with small pulse height in each strip.

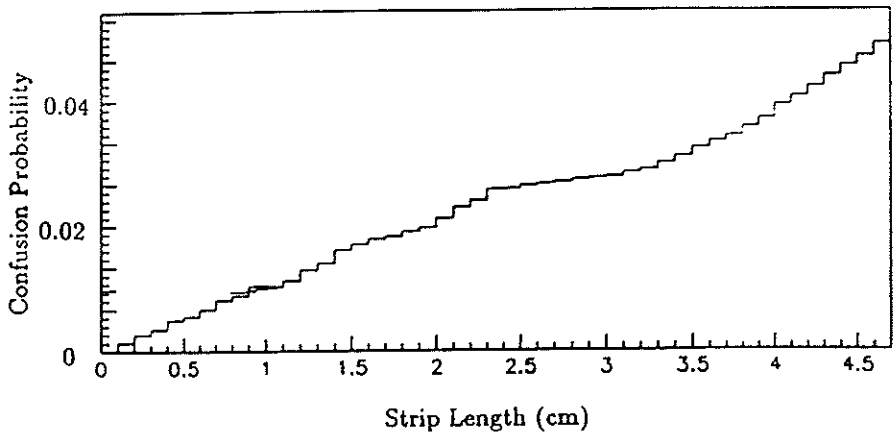

Figure 26: Hit-confusion probability in the barrel detectors as a function of silicon strip length.

there should be two disks per module. The Type B detectors are not actually arrayed in planes, but in a stepped pattern that permits a spiral path for cooling-air flow through the detector. An indication of the offsets of the six Type B detectors per module is shown in the side view of Fig. 27. There are a total of six Type A, six Type B, and six Type C detectors in each inner-hexagon module.

Although it is not part of the present proposal, eventually we would like to build the larger modules shown previously in Figs. 3-5. Such modules have three barrel layers, and require two additional detector types, shown in Fig. 29. Two Type E detectors lie along each face of the outer hexagonal prism, as a single full-length detector could not be made out of a 4″ wafer. It requires a total of 42 detectors to build one large hexagonal module.

We now discuss the various steps needed to bring the inner-hexagon modules into existence.

3.1 Design of the Type A, B, and C Detectors

DC-coupled detectors of the size and shape of Type C have already been fabricated for us by Micron Semiconductor, and tested as described in Secs. 2.3 and 2.4. Production of AC-coupled Type C detectors is well underway, and a first fabrication run was made in Summer 1991. The second run, now in progress, incorporates an improvement to the metallization of the 'foxFET' gate which controls the reverse-bias current. While two Type C detectors can fit on a 4″ wafer, a single one can fit on a 3″ wafer, which we plan to use in this case only.

The Type A and B detectors can be placed on a single 4″ wafer to save on the cost of the mask sets. The design for the Type A, and B detectors will begin in early 1992, with first production in Spring 1992. A large order for a total of 54 Type A, B, and C detectors (18 each) could be placed at the beginning of FY93. This would provide enough detectors for three modules, assuming no damage in construction, or more practically, two complete inner-hexagon modules.

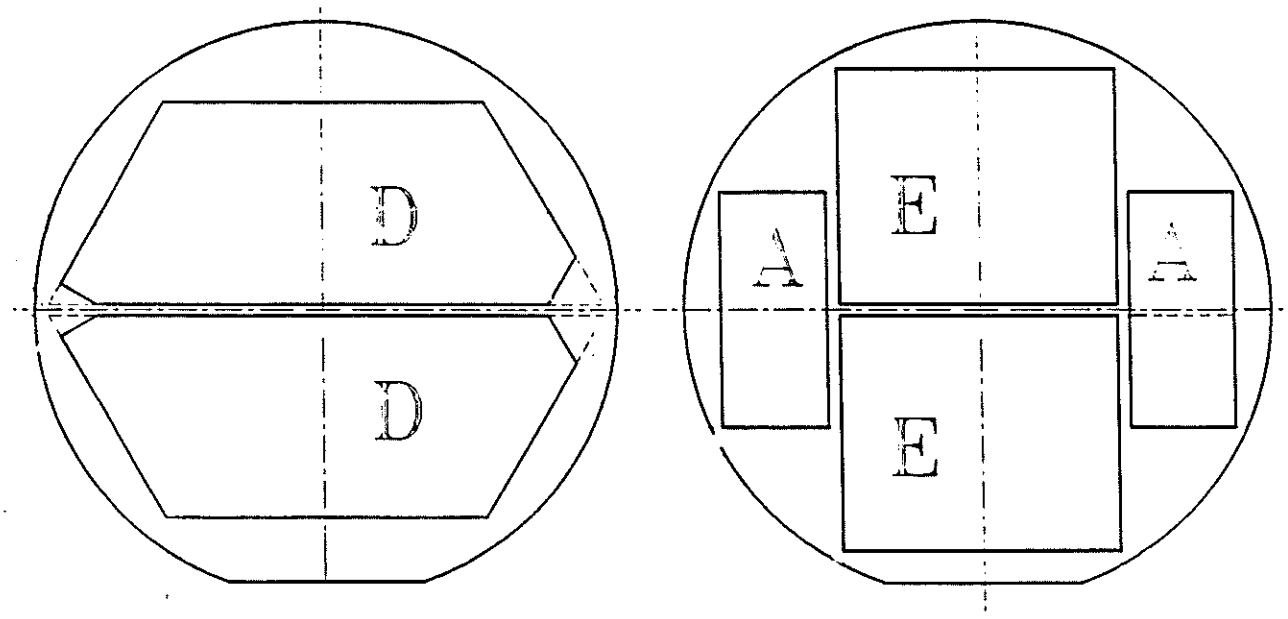

Figure 29: Type D, and E silicon detectors, shown relative to a 4″ silicon wafer. Extra Type A detectors could be incorporated on the Type E wafer to provide test detectors.

3.2 SVX Chip Carriers

Each inner-hexagon module requires 240 128-channel SVX chips to be completely instrumented. There are thus 30,720 channels per inner-hexagon module.

While the SVX chips are now readily available, we must develop a suitable carrier for these chips. The carrier will be glued to a silicon detector, and a row of SVX chips glued to the carrier. The carrier serves to distribute the DC power to the row of chips, and to provide a bus of digital-control and analog-output lines. A custom cable is attached to one end of each chip carrier to connect the chips to the external readout and power circuitry. The chip carrier can also serves as a heat sink to decrease thermal gradients in the SVX chips.

Chip carriers of much of the desired functionality have been developed by CDF for their barrel vertex detector [24]. However, these are physically larger than are suitable for mounting directly on the Type A, B, and C detectors. Also, it would be advantageous to make the chip carriers from aluminum nitride, rather than alumina, because of the superior thermal conductivity of the former. For this we propose to undertake a development program with Promex (Santa Clara).

3.3 Custom Cabling

To bring power and control onto the SVX chips, and the data off them, we need to develop a set of flexible low-mass cable, each having 16 130-Ω pairs of signal lines and 4 DC-power strips. These ($\sim$ 30-cm-long) cables must be quite flexible to reach the SVX chip on the inside surfaces of the inner-hexagon module.

These cables run to a PC board close to the inner-hexagon modules, that includes a

4.1 University of Oklahoma

In FY92 we will finalize our design of doubled-sided AC-coupled silicon detectors with Micron Semiconductor, and evaluate the initial production run. We will also develop aluminum-nitride carrier boards, and special cabling from the SVX chips to the readout modules. In FY93 we will complete the production of 54 Type A,B, and C detectors, and attach them, together with the aluminum-nitride carriers to the inner-hexagon modules, which will then be tested in a fixed-target beamline.

1. Permanent Equipment

    1. 5 double-sided AC-coupled Si-strip detectors (Type C) $15k
    2. Masks for Types A and B Si-strip detectors $20k
    3. Production run of 54 Type A, B, and C Si-strip detectors $100k
    4. SVX chips $5k
    5. Development of aluminum-nitride carriers $20k
    6. Production run of 54 aluminum-nitride carriers $10k
    7. Development of custom readout cabling $20k
    8. MAC-IIci computer, CAMAC crate and interface $10k
    9. CAMAC SVX readout modules $15k
    10. NIM crate, hex discri, quad coincidence, gate generator scaler $10k
    11. Waveform generator (Wavetek 20-MHz) $3k
    12. Spectrum analyzer (Tek 2712 or HP 8591A) $10k
    13. Digital oscilloscope (Tek TDS540) $12k

    Total Permanent Equipment $250k

2. Materials, Supplies, and Travel

    1. Assembly fixtures $5k
    2. Glues, solvents $1k
    3. UV lamp $1k
    4. Miscellaneous supplies $10k
    5. Travel $8k

    Total Materials, Supplies, and Travel $25k

    Indirect Costs of 46% on Materials, Supplies, and Travel $12k

3. **Total University of Oklahoma $287k**

5 Personnel

5.1 Langston University

A recent collaboration has begun between Langston U. and U. Oklahoma under the auspices of the Prairie View Detector Center funded by the Texas National Research Laboratory Commission. D. Gunter and I. Husein and undergraduate students will participate in this project. Initial work will concentrate on testing silicon detectors and readout circuits under the direction of G. Kalbfleisch of U. Oklahoma. This initiative will constitute the first steps in bringing Langston U. into the high-energy-physics-research community.

5.2 University of Oklahoma

In FY92 a new graduate student, T. Vaughn, will join the O.U. silicon effort. Additional graduate students are expected to join in mid 1992 as J. Kuehler and M. Wood move on to their Ph.D thesis projects. A new Postdoctoral Research Associate will be hired in FY92 using funds from the TNRLC. Assistant Prof. P. Gutierrez will continue to be partially involved. This R&D project will continue to be a major component of Prof. G.R. Kalbfleisch's research program.

5.3 Princeton University

J.G. Heinrich and C. Lu will work full time on R&D for SSC subsystems. K.T. McDonald will spend 90% of his research time in these projects. Graduate students W.S. Anderson, and one other to be named shortly will devote all their research effort to this project. In addition, we benefit from access (at no cost to the SSC) to the technical staff of the Princeton High Energy Physics group which includes 1 mechanical engineers, 3 mechanical technicians, 1 electrical engineer, and 3 electrical technician. All salaries of the above people are supported by the DoE HEP Division, except for K.T. McDonald (academic year salary from Princeton University), and W.S. Anderson (NSF Predoctoral Fellow).

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