Summary of Major Detector Working Group
BCD

Kirk MacDonald

Workshop on Major SSC Detectors

Tucson, Arizona

February 18-23, 1990

SSC-240

October 1, 1989

Bottom Collider Detector (BCD)

An Intermediate- and Low-P_t Detector for the SSC

BCD Collaboration[1]

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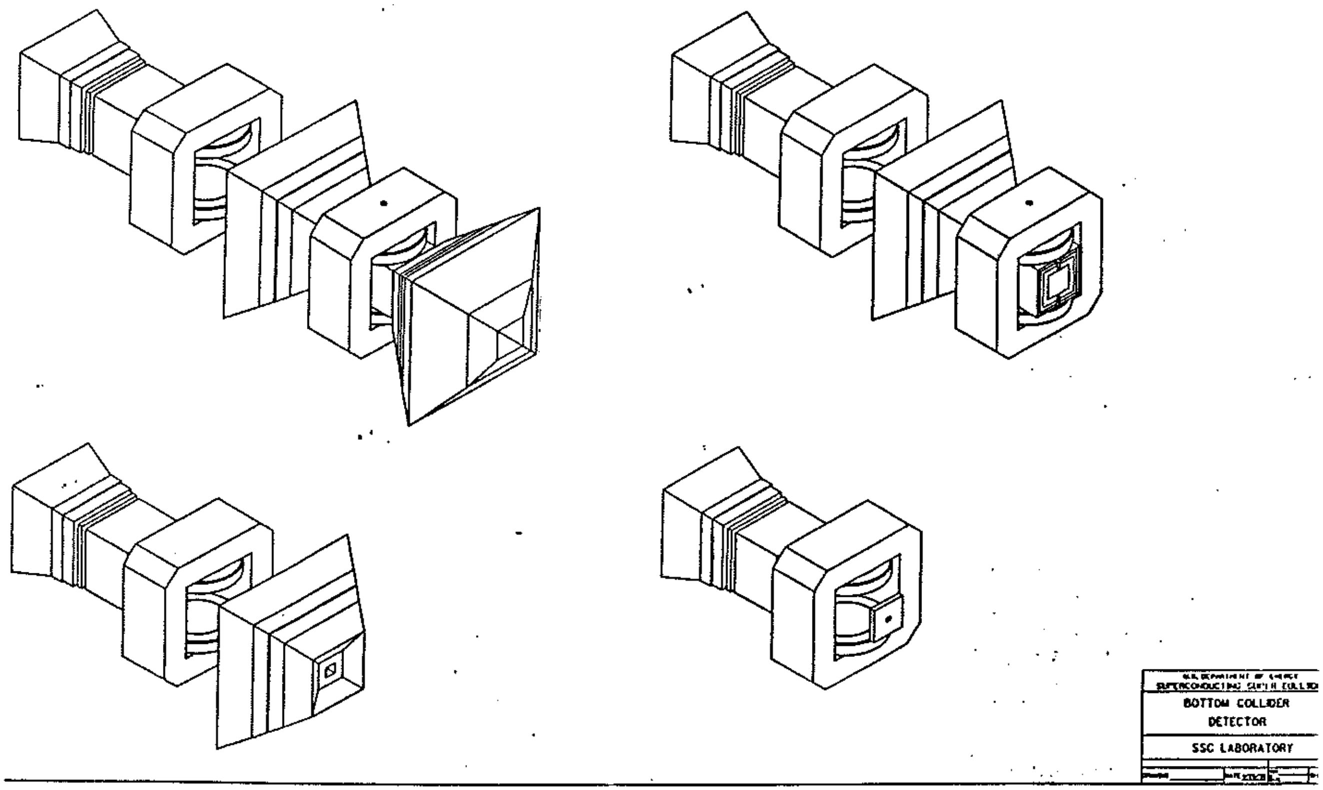
D. Judd, D. Wagoner, *Prairie View A&M U.*
J.G. Heinrich, C. Lu, D.R. Marlow, K.T. McDonald, M.V. Purohit, *Princeton U.*
A.M. Lopez, J.C. Palathingal, *Universidad de Puerto Rico*
B. Hoeneisen, *Universidad San Francisco de Quito*
S. Shapiro, *Stanford Linear Accelerator Center*
M. Sheaff, *U. Wisconsin*
P.E. Karchin, A.J. Slaughter, *Yale University*



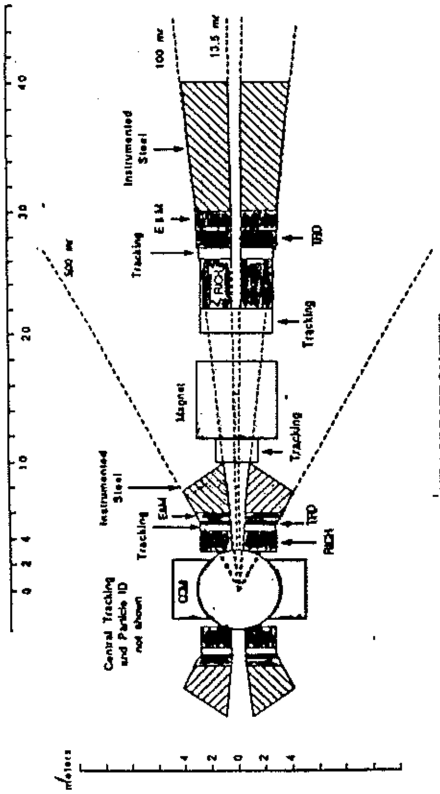


Figure 3: The Snowmass '88 *B* detector.

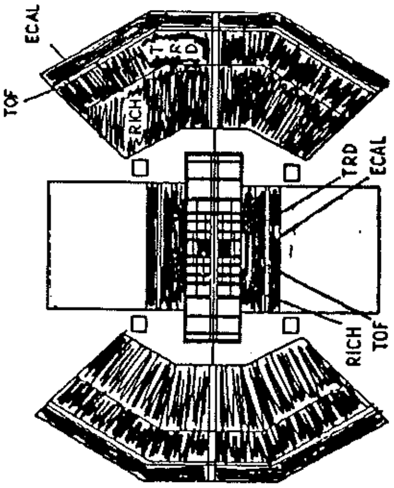


Figure 4: GEANT model of the central part of a *B*-physics experiment; (without the muon identifier).

3 The BCD Detector

3.1 Introduction

As discussed in Section 2, the most interpretable signals of CP violation in the B-$\bar{B}$ system are in the decays of B^0's to a CP eigenstate. To exploit this information it must be determined whether the parent was a B or a $\bar{B}$, which requires 'tagging' of the second B in the event. Hence the experiment must be capable of reconstructing pairs of B-mesons with high efficiency.

Such considerations lead to a detector architecture containing 11 subsystems:

1. **A large dipole magnet** with field transverse to the beams. This can be thought of as the limit of two large-aperture forward spectrometer magnets as the distance between them goes to zero. As a bonus, good central coverage is obtained.
2. **The Silicon Vertex Detector,** with silicon as close as 1.5 cm to the beams.
3. **The Tracking System.** It is too costly to perform all tracking in silicon detectors, so these must be supplemented with tracking chambers, composed of straw-tube detectors in the current design.
4. **The Very Small Angle Fiber Tracking System,** a fast tracking system designed to measure tracks at rapidities beyond those covered by the main detector. It provides a minimum bias trigger, luminosity measurements, and a fast method of determining the longitudinal location of the primary vertex to within ± 1 cm.
5. **Ring-Imaging Čerenkov Counters and Time-of-Flight Counters** to provide identification of charged pions, kaons, and protons.
6. **Transition Radiation Detectors** to provide identification of electrons vs. pions, in conjunction with item 7.
7. **An Electromagnetic Calorimeter,** to complete the electron identification and to provide a trigger and tag on the decays $B \to eX$.
8. **A Muon Identification System** via instrumented steel, covering $|\eta| > 1$.
9. **A Fast Trigger** to reduce the event rate by a factor of 50 before the event information is moved off the detector.
10. **A Barrel-Switch Event Builder** capable of organizing the data streams from 10^5 events per second into individual events.
11. **An online Processor Farm** of about 10^6 MIPS (= 1 TIP) capability to provide the higher-level triggering needed to reduce the event rate to 1000 per second for archival storage.

A view of this detector concept is shown in Figure 2. In the remainder of this section we expand on some of the design considerations of BCD.

Heat Resistance and Air Pressure Drop in a Model of the BCD Silicon Vertex Detector

Hans Jöstlein and Jacqueline Miller

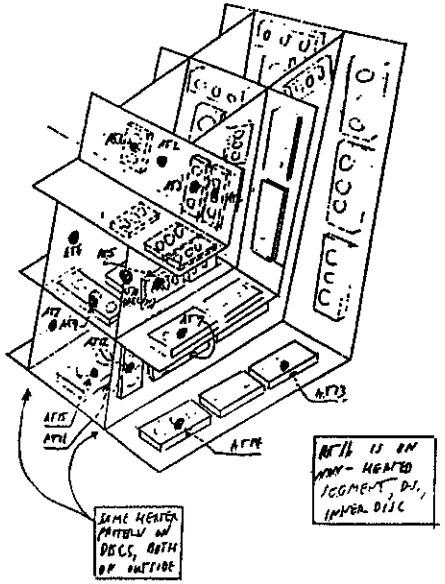


Fig. 4 Placement of the heaters and thermometers on the instrumented module

We have measured both the heat transfer from simulated amplifier chips to the cooling air and the pressure drop per module on a fairly realistic model of part of a large silicon tracking detector for the BCD experiment.

The observed temperature rises are quite moderate, about 10 K in the worst locations. The air flow used may be on the low side if total air temperature rise needs to be reduced (see TM Ref.1). In that case, the heat transfer will get even better.

The total pressure needed to drive the cooling air is 12 inches of water for the 76 g/s flow used here. This flow may be on the low side of what will be needed, depending on the total air temperature rise allowed. The pressure presents, however, no serious technical challenge. Cables will add as yet unknown restrictions to the air flow, which were not modeled here.

Fermilab

TM-1627
October 16, 1989

PROPOSED METHOD OF ASSEMBLY FOR THE BCD SILICON STRIP VERTEX DETECTOR MODULES

Carl Lindenmeyer
Research Division
Mechanical Department

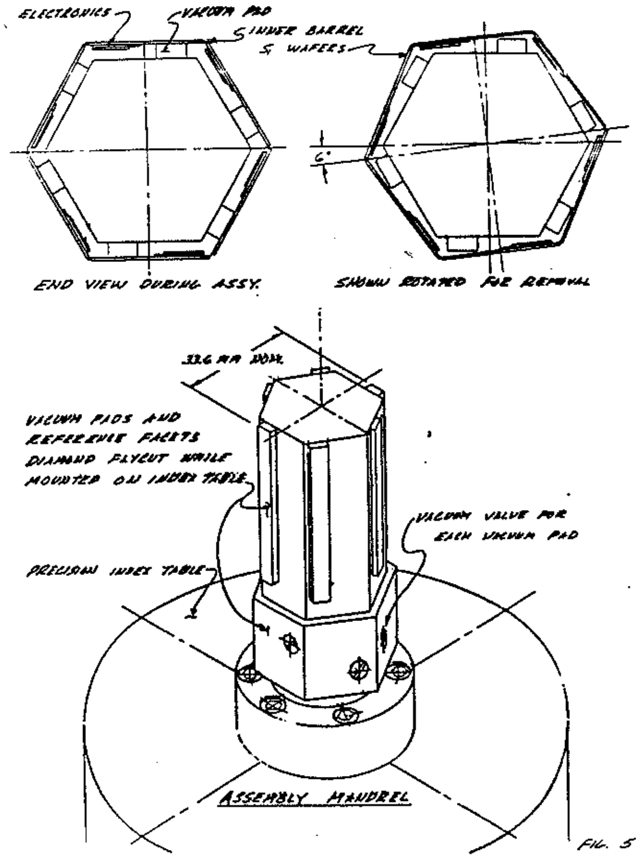


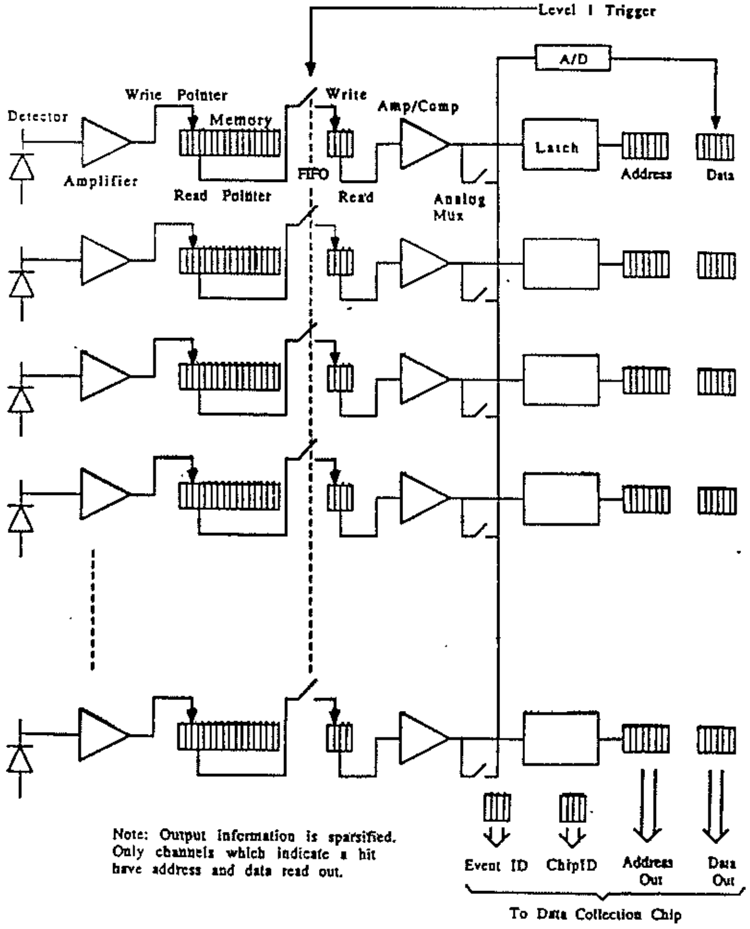
FIG. 5

BVX Workshop Summary

R. Yarema
11/28/89

A workshop was held on 11/8 and 11/9 to discuss the BVX chip design. In attendance were participants from ORNL, LBL, University of Pennsylvania, Yale and Fermilab.

Extremely Simplified BVX Diagram



Note: Output information is sparsified. Only channels which indicate a hit have address and data read out.

CHALLENGING REQUIREMENTS FOR VERTEX TRACKING DETECTOR

HUGHES
9936-PP/8 MCSS

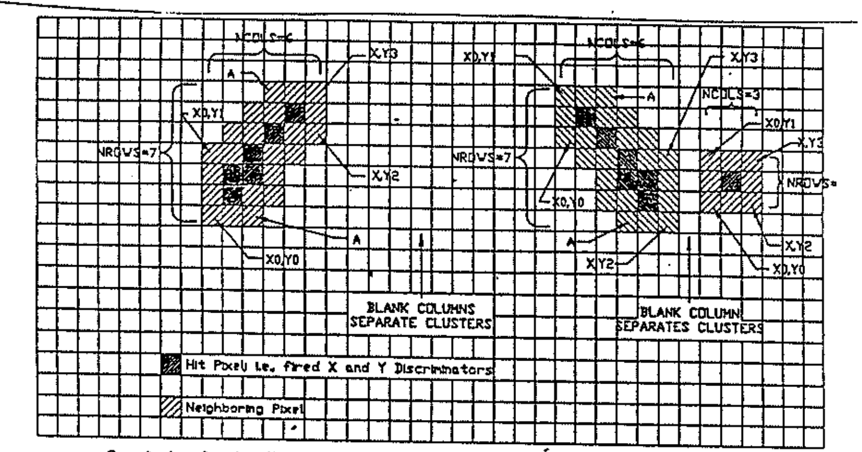
NO. OF PIXELS = 10^7
PIXEL SIZE = 30μm x 30μm
NOISE LEVEL = 50 ELECTRONS RMS
TAG TIME PER HIT = 15 NANO SECONDS
READOUT TIME = 1 MICROSECOND
RADIATION HARDNESS = 1–10 MRAD
HYBRID THICKNESS = 500 MICRONS

11/10/89

NEAR TERM PIXEL READOUT REQUIREMENTS DEFINITION

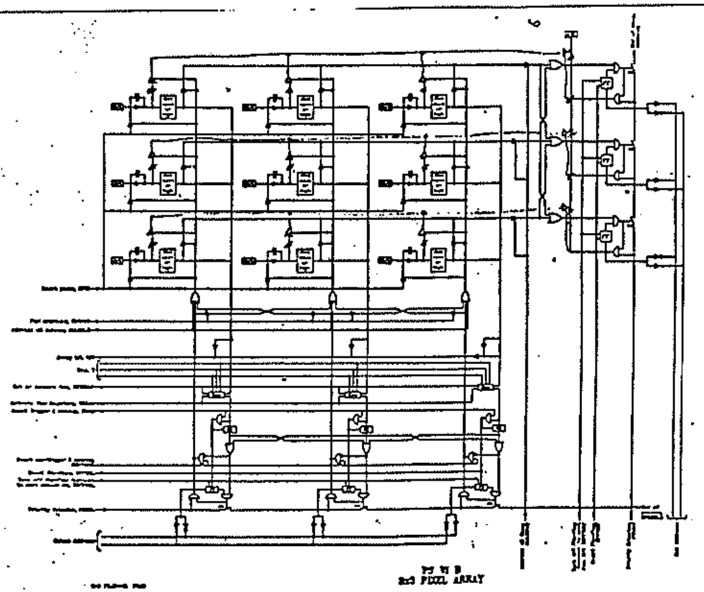
HUGHES
9946-MD8 MCSS

ARRAY SIZE = 256 x 256/N
PIXEL SIZE = 30μm x 80μm x N
TAG TIME = 15ns
READOUT TIME = 500nS/HIT
RADIATION HARDNESS = > 500K RAD
NOISE LEVEL = 200 ELECTRONS RMS
UNIT CELL FUNCTIONS = AMPLIFICATION
ANALOG BITS = 5 – 8
PERIPHERAL CIRCUIT FUNCTIONS = TIME REGISTER, FAST SCAN PATTERN MATCHING
POWER = 10μW/PIXEL



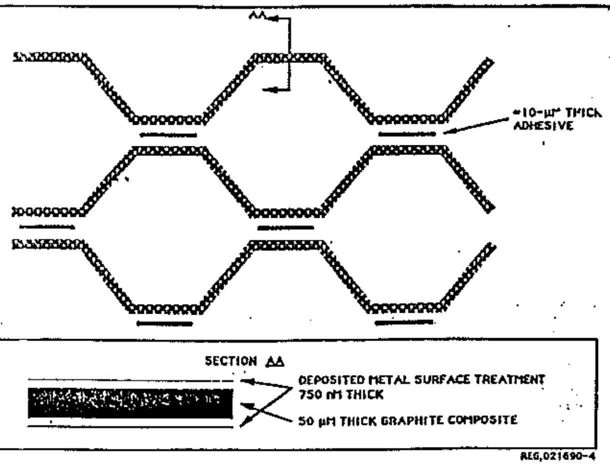
Coordinates found in the sample DSP program are X0, Y0, Y1, Y2, Y3, X, NCOLS, NROWS, but coordinates of pixels labeled 'A' can also easily be found.

Other quantities calculated by DSP for determing centroid are XV, YV, V.



PRESENTED BY RAY GARVEY
APPLIED TECHNOLOGY DIVISION
OAK RIDGE NATIONAL LABORATORY*

COMPOSITE STRAW BUNDLES



DOE/ER/3072-56
December 7, 1989

PROTOTYPE STUDY OF THE STRAW TUBE PROPORTIONAL CHAMBER

C. Lu, K.T. McDonald and D. Secrest
Joseph Henry Laboratories, Princeton University, Princeton, NJ 08544

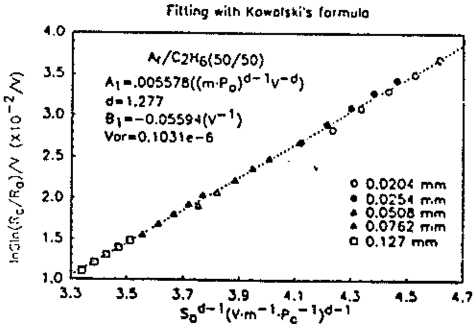


Fig. 5. *Model fits to the gas gain in Ar/Ethane (50/50) gas.*

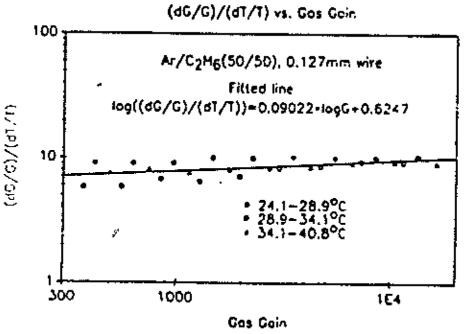


Fig. 6. The ratio of relative gain change (dG/G) to the relative temperature change (dT/T) as a function of the gas gain in P-10 and Ar/Ethane (50/50) for 0.8-mil and 5-mil diameter anode wires.

Table 2. A sample of wire instability measurements.

T (gm)	V (V)	Measured displacement of anode wire D_{wire} (mm)	V_0 (V)	$(V_0/V)^2 - 1$	Calculated displacement of the tube D_{tube} (mm)
20	0	0	1718		
	800	0.063		3.61	0.225
	900	0.13		2.64	0.336
	1000	0.16		1.95	0.310
	1100	0.22		1.44	0.320
	1200	0.32		1.05	0.333
	1250	0.38		0.89	0.339
	1300	0.51		0.75	0.379
	1350	unstable			

HIGH-SPEED BIPOLAR INTEGRATED CIRCUITS FOR SSC APPLICATIONS

F.M. NEWCOMER, R. VAN BERG, J. VAN DER SPIEGEL and H.H. WILLIAMS
University of Pennsylvania, Philadelphia, PA, USA

Table 1
Design parameters for preamp/shaper

Noise	< 2000 rms electrons E.N.C.
Power	5–20 mW per channel
Dynamic range	2–8 bits dependent on sensor type
Input impedance	100–200 Ω optimize for chamber impedance
Rise time	3–5 ns to minimize timing jitter
Double pulse resolution	< 20 ns
Packing density	4–16 channels/cm^3

A Fast Low-Power Time-to-Voltage Converter for High Luminosity Collider Detectors

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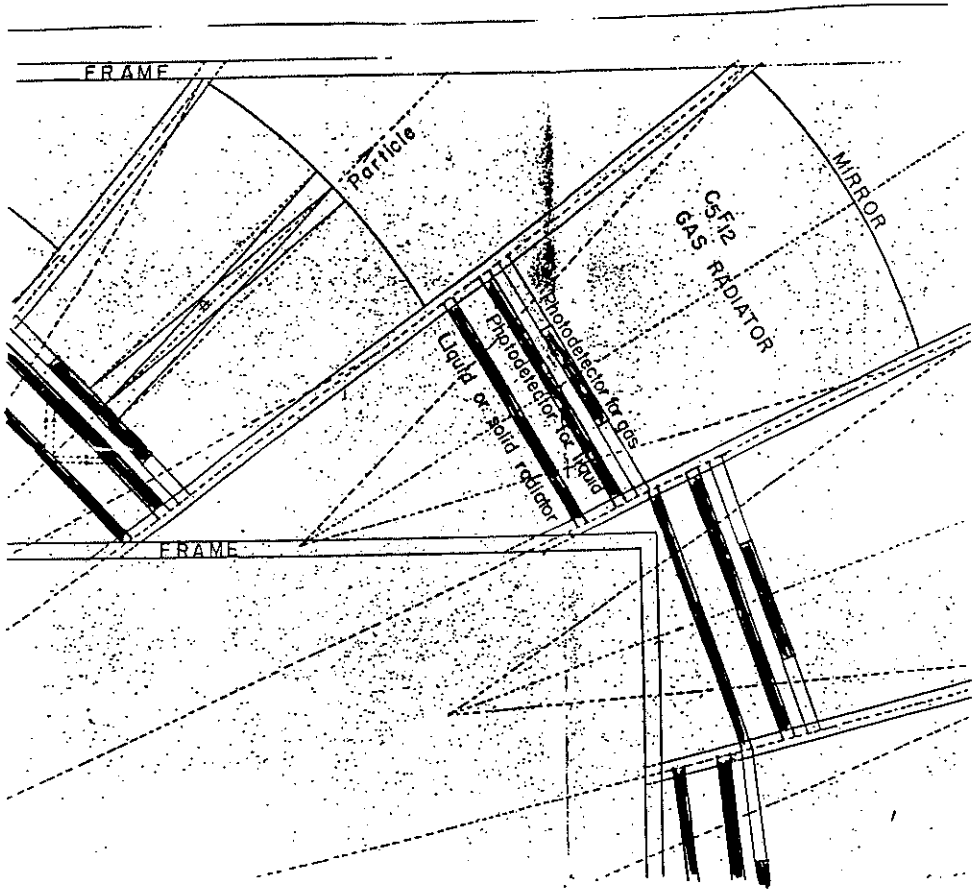
V. BUDIHARTONO, R. P. VAN BERG, J. VAN DER SPIEGEL, H. H. WILLIAMS
University of Pennsylvania, 209 S. 33rd St., Philadelphia, PA 19104

L. CALLEWAERT, W. EYCKMANS, W. SANSEN
Catholic University of Leuven, Kardinaal Merdierlaan 94, Heverlee, Belgium

Abstract—A new CMOS integrated circuit has been designed to measure the time interval between two digital voltage pulses. The measurement is stored as an analog voltage on a capacitor for later digitization. The targeted range of measurable times is 5–25 nanoseconds, with a resolution of 0.5 nanoseconds. An additional feature of the circuit is a storage depth of 8 samples, i.e. 8 consecutive time measurements may be recorded individually. Hence, the chip is a combination of a time-to-voltage converter (TVC) and an analog memory.

REPORT #6 ON THE BOTTOM COLLIDER DETECTOR: PRELIMINARY DESIGN OF THE RING IMAGING CHERENKOV DETECTOR

Bruce Hoeneisen
Universidad San Francisco de Quito



OPTIMISATION OF THE TRANSITION RADIATION DETECTOR

Angel M.Lopez
and
Jose C.Palathingal

Department of Physics
University of Puerto Rico
Mayaguez
Puerto Rico

10 MODULES , ~3 CM THICK
~137 CH_2 FOILS/MODULE , 12μm THICK
⇒ X-RAY PEAK ~5 KeV ⟺ Ar + Kr GAS
~1 DETECTED X-RAY MODULE
READOUT : PIXELS VS. STRIPS ?

E-M CALORIMETRY

DAVE ANDERSON : COMBINED Č + SCINTILLATION

PbF : ρ=8 $X_0 = 9_{mm}$ Č SOURCE = FAST (<1ns

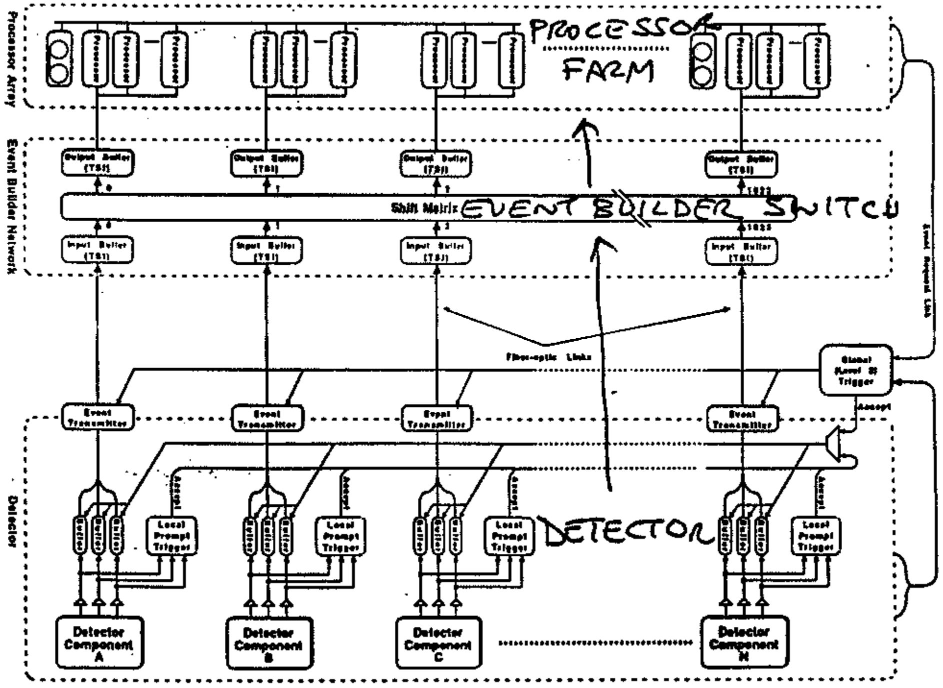
+ TbF SCINTILLATOR (LOW CONCENTRATION) = SLOW (~15n

SEPARATE e/π BASED ON $\frac{\text{FAST}}{\text{SLOW}}$ COMPONENTS

READOUT : PHOTOMULTIPLIER (~1300 PHOTO e / GeV)

A HIGH-THROUGHPUT DATA ACQUISITION ARCHITECTURE BASED ON SERIAL INTERCONNECTS

M. Bowden, H. Gonzalez, S. Hansen, A. Baumbaugh
Fermi National Accelerator Laboratory
Batavia, Illinois 60510



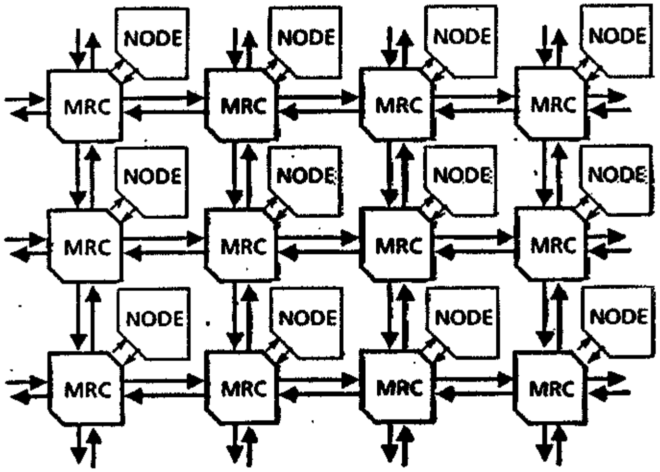
Generalized Data Acquisition System Architecture

Data Acquisition System Goal:

**Open System Architecture
For The Online Processor Farm**

Open System Architecture...Any commercial or in-house built online farm can be used in the Data Acquisition Syste

SSC Processing Farm - 1994



2D (3D) mesh topology

wormhole routed

scalable to 4K (65K) nodes

low latency (40 ns/hop)

high bandwidth (>100 MB/s)

self-timed design

MRC **a VLSI mesh router chip (MRC)**

4096 Processing Nodes
@ 250 × VAX-11/780 ea.
Total Power = 1 megaVUPS

Initial Experience with the Intel i860 Microprocessor

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University of Pennsylvania, Philadelphia, Pa. 19104

J. G. Heinrich and K. T. McDonald
Joseph Henry Laboratories, Princeton University, Princeton, N.J. 08544

January 13, 1990

Our results for the various programs of the standard benchmark suite follow:

Program	Result
Dhrystone V1.1	64000 dhrystones/second
Dhrystone V2.1	52000 dhrystones/second
Single P. Whetstone	24000 whetstones/second
Double P. Whetstone	19000 whetstones/second

Our results for the crude benchmark using ISAJET follow. Note that the result for the Amdahl was taken during the day with users on the system.

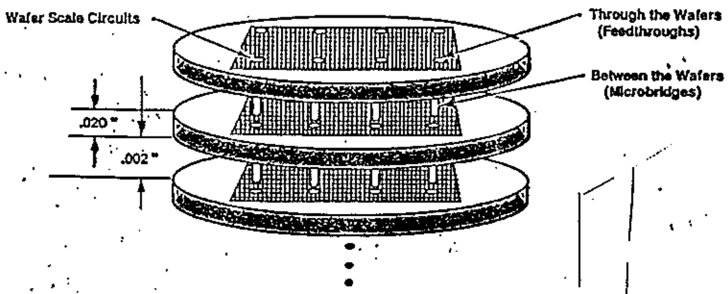
Machine	Result (sec)
Vax 3100	409
Dec 3100 (16MHz)	129
Amdahl	110
i860	101

3-D COMPUTER

HUGHES

C17820-1R1

1987



FEASIBILITY DEMONSTRATED

- 5 WAFER STACK
- 32 x 32 ARRAY OF PROCESSORS
- CONTROL UNIT
- SYSTEM SOFTWARE
- SOME APPLICATION SOFTWARE

2×10^7 OPERATIONS/sec
1.3 WATTS
8 inches^3

1990

INTERMEDIATE 3-D COMPUTER

- CURRENT AIR FORCE CONTRAC
- 15 WAFER STACK
- 128 x 128 ARRAY
- SUN WORKSTATION

10×10^9 OPERATIONS/sec
<100 WATTS
<20 inches^3

1994

FINAL 3-D COMPUTER

- 25 WAFER STACK
- 512 x 512 ARRAY

1×10^{12} OPERATIONS/sec
<500 WATTS
<100 inches^3

BCD IN 1990

- EOI TO SSC
- BEAM TESTS IN M-TEST @ FERMILAB
  - SILICON DETECTORS: AC & DC COUPLED STRIPS
    HUGHES PIXEL ARRAY
  - READOUTS: SVX, CAMEX
  - STRAW TUBES: ∼800 W/LOW-MASS END STRUC
  - READOUT: PENN/ATT BIPOLAR
- SIMULATION: ISAJET/GEANT + PATTERN RECOGNIT.
  - SILICON VERTEX, STRAWS, RICH, TRD, E-M CAL
  - ⇒ LOTS OF CPU TIME!!
  - TRIGGER: e's; SECONDARY VERTEX; 'TOPOLOGY'
- R&D
  - ABOVE SYSTEMS + RICH, TRD, E-M CAL,
    EVENT-BUILDER SWITCH
- FUTURE BEAM TESTS IN C0 @ FERMILAB
  - ⇒ B-PHYSICS AT ENTRY LEVEL