Design of the local trigger board for the Daya Bay reactor neutrino experiment

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A B S T R A C T

We have designed a local trigger board for the Daya Bay reactor neutrino experiment, which is aimed to measure the neutrino mixing angle $\sin^2 2\theta_{13}$ with a precision down to 1% level. The local trigger board processes both the total number of coincident photomultiplier tube (PMT) hits and the PMT energy sum to make trigger decisions. With this design, a high trigger probability is achieved to meet the system requirement. The design of the local trigger board is presented.

1. Introduction

Measuring the mixing angle $\sin^2 2\theta_{13}$ down to 0.01 or better is very challenging at reactor neutrino experiments. However, this 1% level precision is very crucial in understanding the physics beyond the standard model and in guiding future experiments for studying Charge–Parity (CP) violation in the lepton sector \cite{1}. Current knowledge on $\theta_{13}$ is $\sin^2 2\theta_{13} < 0.17$ for $\Delta m^2_{31} = 2.5 \times 10^{-3}$ eV\(^2\) obtained by CHOOZ \cite{2}. Many approaches are now underway \cite{3–6}. Since the measurement of $\theta_{13}$ using reactor neutrinos suffers less complication from the other mixing angles, it is believed to be capable of providing the best sensitivity.

The Daya Bay reactor neutrino experiment \cite{3} aims to achieve this goal, taking advantage of 17.4 GW of thermal power from three pairs of reactor cores (Daya Bay, Ling Ao I and Ling Ao II) and the adjacent mountainous terrain. The basic experimental layout of Daya Bay consists of three underground experimental halls, one far and two near linked by horizontal tunnels, with baselines of 1800 and 400 m to the reactor cores respectively. Three types of sub-detectors are employed as shown in Fig. 1: the anti-neutrino detector (AD) with the liquid scintillator doped with gadolinium (Gd), the water Cherenkov detector (MUON) and the resistive plate chambers (RPC). The first detector is used to detect the anti-neutrino signal. The last two are used to detect the cosmic ray background, which needs to be rejected. The far site consists of four ADs, one MUON and one RPC, while each near site consists of two ADs, one MUON and one RPC.

In the 0.1% Gd doped liquid scintillator target, the signature is an anti-neutrino interaction with proton, producing a prompt positron with continuum energy distribution from 1.02 to 10 MeV and a thermal neutron:

$$n + p \rightarrow e^+ + n$$

(1)

During the process of collision with the atoms about 85% of neutrons will be captured by Gd and release 8 MeV delayed cascade $\gamma$ with an average capture time of 28 $\mu$s. The rest of neutrons will be captured by Hydrogen and release 2.2 MeV delayed $\gamma$ with an average capture time of 180 $\mu$s. The interaction requires the trigger system to be able to detect both the prompt positron and the delayed neutron with minimum acceptance loss. As the key module of the trigger system, the local trigger board (LTB) should have high trigger probability ($> 99\%$). The design and the test results of the LTB will be discussed in the following sections.

2. Overview of the trigger system

Fig. 2 shows the connections between sub-detectors and electronics. Since both the AD and the MUON employ the PMTs, identical front-end electronics board (FEE) \cite{7} and LTB are used for both to facilitate the design and on-site maintenance. In the
sources, the LTB can generate the final trigger decision signals: the local trigger to the FEEs and the cross trigger to the MTB. The MTB is used for the communication between the LTBs. With the MTB, the external calibration trigger request used to monitor the detector performance and the cross trigger generated by any single LTB can be broadcasted to the correlative LTBs.

The RPC sub-detector uses specific front-end electronics with self-trigger scheme, which will not be discussed in this paper.

3. LTB hardware

As shown in Fig. 3, the LTB is designed as a 9U VME standard slave module [8], mainly consisting of a clock circuit, a field programmable gate array (FPGA) chip, a NHIT process circuit, an energy sum process circuit, LVPECL (low-voltage positive emitter-coupled logic) transceivers and an FPGA configuration circuit.

3.1. Clock circuit

The clock circuit receives a 40 MHz clock from the clock system and outputs two identical zero delay 40 MHz clock signals via a clock generator. One clock output is fed to the LTB FPGA directly. The other one is fed to all the FEEs in the same crate via a fan-out board. In the case of no clock system, an on board 40 MHz crystal oscillator can be conveniently enabled via a jumper.

3.2. FPGA

All the trigger decision logics are implemented by the FPGA chip. Considering the possible resource consumption, a Virtex4 serial FPGA XC4VLX25-10FF668C from Xilinx [9] is chosen. It is estimated that the present trigger decision logic consumes about 25% of FPGA resource, leaving sufficient margin for future improvement of the trigger decision logic.

3.3. NHIT process circuit

The number of coincident PMT hits of each FEE’s PMT group with a valid value from 0 to 16 is transmitted to the LTB over a

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**Fig. 1.** Daya Bay reactor neutrino experiment detector.

**Fig. 2.** Overview of the trigger system.

**Fig. 3.** Simplified block diagram of the LTB hardware.
6 LVDS links running at 80 MHz, which consist of one clock link and 5 data links. In total, 96 LVDS links are used to transmit the NHITs from all 16 FEEs.

3.4. Energy sum process circuit

The energy sum (ESUM) circuit receives and sums over 16 groups of energy pre-sums from the FEEs, as shown in Fig. 4. To reduce noise and cross talk, the energy pre-sum is transmitted as differential analog signal between the FEEs and the LTB. The 16 energy pre-sums are divided into two parts of 8 inputs. By averaging those two parts two half energy sums are generated. By averaging two half energy sums further, the total energy sum is generated. Then three energy sum signals are shaped and discriminated. The adoption of the average algorithm can avoid the saturation of the energy sum. In this design, even if one problematic PMT channel introduces high level noise to one half energy sum, the other half energy sum can still be unaffected. To increase the discrimination accuracy, a baseline restoration circuit is used when summing up the energy pre-sums.

After discrimination, three over-threshold pulses are sent to the FPGA. The thresholds of the three discriminators are set via a DAC chip controlled by the FPGA. In addition, one of the three shaped energy sum signals can be selected via an analog multiplexer and fed to an on board 10 bit 40 MSPS ADC chip. The output data of the ADC chip is also sent to the FPGA to make the trigger decision via a digital discrimination scheme. The ADC output data can be cross-checked with the over-threshold pulses.

To monitor the energy sum circuit, one shaped or unshaped energy sum signal can be selected via a multiplexer and sent to an external flash ADC module.

3.5. LVPECL transceivers

LVPECL is a differential signaling standard and mainly applied in high speed circuits. On the LTB, MAX9375 is selected as the LVPECL transceiver to interface the time signal, the clock signals and the trigger signals as well.

3.6. FPGA configuration circuit

The LTB uses a Complex Programmable Logic Device (CPLD) and a FLASH memory to configure the FPGA online. The FPGA configuration data are written into the FLASH memory via the VME interface logic implemented in the CPLD chip. The CPLD can read the configuration data from the FLASH memory and configure the FPGA in a slave serial mode automatically after being powered up or receiving a configuration request from the VME controller. This feature ensures that the FPGA firmware can be updated remotely.

4. LTB firmware

The trigger decision logics are implemented by the firmware loaded in the FPGA as shown in Fig. 5.
4.1. Clock and time stamp

The FPGA receives a 40 MHz clock from the clock circuit. In order to reduce the trigger latency, the trigger decision logic works at 80 MHz clock, which is generated by the on-chip Phase Locked Loop (PLL).

Absolute time information is distributed to the LTB via a single serialized input signal every second. This time information is encoded in an IRIG-B format [10] and carries year, month, day, hour, minute, second and a high precision Pulse Per Second (PPS) signal. Inside the FPGA, the IRIG-B signal is first decoded and stored in registers. The PPS signal is used to reset a free running 80 MHz tick counter. This counter is latched when a trigger decision is made to provide the time information inside 1 s as the number of 12.5 ns slices since the rising edge of the last PPS signal. This counter, together with the year, month, day, hour, minute and second information in the registers, forms the whole time stamp for each trigger event.

4.2. Trigger decision

The LTB has 10 trigger sources: multiplicity trigger, 4 types of ESUM triggers, cross trigger, calibration trigger, periodic trigger, software trigger and random trigger.

The multiplicity trigger is generated by summing up all the NHITs and discriminating the NHIT sum. Three types of ESUM triggers (total ESUM trigger, low ESUM trigger and high ESUM trigger) are generated by processing three ESUM over-threshold pulses, while another ESUM trigger is generated by discriminating the ADC data. The cross trigger and the calibration trigger are received by decoding the serial encoding trigger requests from the MTB. The periodic trigger, the software trigger and the random trigger are generated internally. Most of the triggers can be delayed with a programmable latency to synchronize with each other.

From these 10 trigger sources, two sets of trigger sources can be selected via VME bus. One set of trigger sources are OR'ed to generate the raw local trigger, while the other set of trigger sources are OR'ed to generate the raw cross trigger.

To guarantee that the FEEs can receive the local trigger correctly and have enough time to acknowledge the trigger, the raw local trigger will be regulated, as shown in Fig. 6. The following raw local triggers covered by the regulation window are masked without regulation. To facilitate the offline analysis, the detailed information of all raw local triggers covered by the regulation window is recorded including the trigger type, the time stamp and so on. According to the requirement of the FEE, the width of the regulation window is about 500 ns and the width of the regulated trigger pulse is about 100 ns, both of which can be configured via the VME bus. At the end of the regulation window, all trigger information is packed into a trigger data package, which is buffered in FIFOs for VME read.

The LTB checks both the LTB data buffer and the FEE data buffer to avoid overflow. If any data buffer is almost full, the regulated local trigger and the corresponding data package will be blocked. The number of blocked triggers is recorded and can be used to analyze the dead time of the trigger system.

The raw cross trigger is similarly regulated to generate the cross trigger, which is sent to the MTB and then broadcasted to the other related LTBs.

4.3. VME interface

A VME slave interface is implemented on the LTB, which supports both the single word access mode and the Chained Block Transfer (CBLT) mode [11]. Plenty of control and status registers are created inside the FPGA to control and monitor the trigger decision logic. In addition, plenty of Random Access Memory (RAM) blocks are also employed inside the FPGA to monitor the interim data generated at each stage of the data processing. These registers and RAM blocks are accessible in the single word access mode. Compared with the single word read, the CBLT read is much faster and is specially used to read the trigger data packages.

5. Test of the LTB

In order to test the LTB hardware and firmware more conveniently, a dedicated trigger test board (TTB) is developed. This test board has the same dimension, adopts the identical FPGA chip as the LTB and works as a VME slave module as well in the same crate with the LTB. The TTB can generate 16 differential analog signals, 16 digital signals and clock signal to feed the LTB. Based on this test board, a test system is set up as shown in Fig. 7. As physical triggers, the ESUM trigger and the multiplicity trigger are tested.

Under a certain threshold, the total ESUM trigger probability as a function of the average amplitude of the 16 analog input

80MHz clock

Masked raw local triggers

Raw local trigger

Regulated local trigger

Regulation Window

Fig. 6. Local trigger regulation scheme.

Fig. 7. Test system.
signals is shown in Fig. 8, which shows that the baseline restoration circuit can sharpen the rising slope of the trigger probability curve. The average amplitude of the 16 analog input signals that can produce a trigger with a probability of 50% is defined as the measured threshold. With the baseline restoration circuit, the trigger probability gets higher than 99% when the average input amplitude is about 1.9% higher than the measured threshold.

The multiplicity trigger probability as a function of the sum of all NHIT input signals with a threshold of 10 hits is shown in Fig. 9. Once the NHIT sum is higher than the threshold, the multiplicity trigger probability reaches 100%; otherwise the trigger probability is zero.

When either the LTB data buffer or the FEE data buffer is full, the trigger will be blocked and a dead time will be introduced. To study the contribution of the LTB to the dead time, the relation between the status of the LTB buffer and the trigger rate is tested by using the random trigger. Without the FEEs, the LTB buffer will not be full with an average random trigger rate up to 150 kHz, which is much higher than the expected trigger rate of the system (about 1 kHz).

The LTB has also been tested with a prototype experiment [12] in which a liquid scintillation detector with 48 PMTs, one LTB, three FEE boards and the DAQ system work together. The prototype experiment has been running smoothly for more than a year and no LTB design failure has been observed.

6. Conclusion

We have developed the LTB for the Daya Bay reactor neutrino experiment. In order to study and achieve high trigger probability, 10 types of trigger sources are implemented in the design of the LTB. These trigger sources are processed independently and simultaneously to generate the final trigger decisions. All the trigger information can be recorded and read out by the DAQ system via a VME interface for the offline analysis. The LTB has been tested with a special test board and the prototype experiment, and proven to work well.

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References