VME SUMMARY INTERLOCK AND ALARM MODULE
VME SIAM

I. Description:

The Summary Interlock and Alarm Module (SIAM)[1] is a VMEbus compatible module which can generate an output signal (trip) based on the latched state of eight input conditions (faults). Several modules can be daisy-chained to form a larger set of input conditions. In its simplest form this is an expandable eight input OR gate.
A block diagram of one SIAM channel is shown in Figure 1.
The module has eight optically isolated inputs which may be connected to sensors or relays which detect error conditions. If an ***error*** lasts longer than a predetermined time it causes a ***fault*** condition which is latched. An ***inhibit***, programmable from either the front panel or the VMEBus, is associated with each input. This inhibit can be set to prevent any channel's fault from generating a ***trip*** state. A jumper selectable option disables this feature to prevent inadvertent inhibit of critical subsystems. A trip state drives the module's Interlock and Alarm (I&A) optically isolated outputs, and the daisy-chain output. A latched fault can be reset from either the front panel or the VMEbus only when the error signal itself has disappeared.
A personality module (mezzanine board) provides programmability via jumpers and resistors to configure each input independently. An input can be connected to either normally open or normally closed contacts (Figure 2), or it can be optically isolated to accept an active high or an active low logic signal (Figure 3). A time constant determines how long an input error signal condition must be present before it causes a fault.
Two optically isolated outputs (Figure 4) labeled I&A-1 and I&A-2 are used to indicate an uninhibited fault condition within the module or within a module located upstream in a chain of modules. For example, one output could be connected to an interlock system and the other one to an alarm system.
The expansion ability to accommodate more than eight inputs is provided by the Daisy-chain input and the Daisy chain output. The Daisy-chain input is TTL compatible, and the Daisy-chain output is a TTL open collector output.
Indicators and a status register are provided for visual and computer monitoring of the module.

II. Mode of operation

Since the bits in the status register duplicate the information presented via front panel LEDs, we will refer only to the LED's status within this section, a lit or flashing LED correspond to a bit set to one in the status register.
The first step in using the SIAM consists of determining what conditions may generate an interlock and/or an alarm for the system being monitored. If eight or less conditions are enough only one module is required. If however, there are more than eight error conditions two or more modules will need to be daisy-chained. A single SIAM system or the first module in a multiple SIAM system must have either its daisy-chain input pulled down to ground, or the Start of Daisy chain

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pin, on the personality module, tied to ground. In a multiple SIAM system the daisy-chain output of the first module is connected to the daisy-chain input of the following module and so forth, the interlock and alarm are, in general, generated by the last module in the chain (the SIAM which detects a fault and all SIAMs located after it in the daisy-chain have their I&A output transistors non conducting (open)).

Next, for each type of sensor the corresponding input needs to be configured for:

- Contact closure or contact break if the module provides the voltage to the sensor
- Active high or active low logic level signal if the voltage is supplied by the sensor (the input is then optically isolated).
- The minimum duration the error condition must be present to generate a trip signal

This is done with resistor selection and jumpers on the personality module as explained in section VI.

In the following example we look at only one module, but a chain of modules will function in a similar manner, the inputs of the first module in the chain look like the inputs of a single module system and the outputs of the last module look like the outputs of a single module system.

Once the above setup is done and the sensors are properly connected to the SIAM, the module will operate as follows.

During normal operation when there is no fault all the green ***OK*** LEDs are lit, and the yellow ***Inhibit*** and red ***Trip*** LEDs are off. If an error occurs the OK LED for that channel is turned off. After the programmed minimum fault time, if the error persists, the Trip LED for that channel flashes on and off, the Daisy-chain output, and the I&A output transistors open. In order to be able to reset the trip condition the error which caused the OK LED to be turned off must be remedied so that the OK LED lights again. The trip condition can then be reset by either depressing the ***Reset/Inhibit*** switch for that particular channel or writing a one in the proper bit of the reset register via the VMEbus (section VII).

When permitted (lock inhibit jumper removed) any channel trip can be inhibited so that it does not generate a system trip condition, thus not changing the state of the daisy-chain, I&A-1, and I&A-2 outputs. This operation is done by either, depressing simultaneously the ***Select Inhibit*** switch and the channel's Reset/Inhibit switch or writing a one in bit 0 of the channel's inhibit register. When a channel is inhibited its functionality is not altered but it will not change the module's Daisy-chain and I&A output signals if an error is detected. This inhibit can be cleared by either, depressing simultaneously the Select Inhibit and the channel's Reset/Inhibit switches or writing a zero in bit 0 of that channel's inhibit register. When the inhibit is set the Inhibit LED for that inhibited channel flashes on and off.

The module can be tested manually or via VME. In the manual mode depressing the Test push-button switch will always cause the Daisy-chain output, and the I&A output transistors to open as long as the switch is depressed. In the programmable mode writing a one to bit 0 of the test register will have the same effect as depressing the Test switch, writing a zero in bit zero of the test register will have the same effect as releasing the Test switch. However, this VME test feature is disabled when the VME Test Disable jumper is installed.

III. Module Specifications:

A. Module type: Single width VME module

B. Input channels: Eight

C. Input levels:

1. User supplied external voltages
   "0" = -30V to +1V
   "1" = +3V to +30V
   Undefined from +1V to +3V
   Input optically isolated with current drawn not to exceed 15 mA at 30V
2. User supplied contacts
   Normally open (NO)
   Normally closed (NC)
3. Daisy-chain In
   TTL with 5kΩ pull-up to +5V

D. Outputs

1. Two identical Alarm and Interlock (I&A-1 and I&A-2): Optically isolated power transistor, TIP120, NPN darlington
   Emitter and collector available as a switch; closed when there is no fault, open when there is an uninhibited trip.
   Ratings:
   Maximum collector voltage: 35V
   Maximum current: 0.5A, collector fused at 1A
   Built-in base emitter shunt resistors and output diode
   At 0.5A collector current, transistor voltage, Vce, is 0.5V
   At 1.0A collector current, transistor voltage, Vce, is 0.7V

2. Daisy chain: TTL Open collector active high signal

E. Latching

Each channel independent of other channels

F. Power required

+5V
+12V
If the +12V line fails, a fault condition occurs

G. Protection

Input withstand +/-30V indefinitely; +/-100V for 30 seconds

IV. Front Panel

A. Front panel indicators

1. VME access green LED
2. For each channel:
   OK green LED
   Inhibit (INH) flashing amber LED
   Trip (TRP) flashing red LED
   When a trip indication is latched the red trip LED will continue to flash on and off even though the fault condition that gave rise to the trip may have cleared.If the fault condition clears, the green OK and the blinking red trip LEDs will both be on. To clear the flashing red LED, the Reset/Inhibit switch for that channel must be pushed, or the corresponding bit in the Reset register set (section VII)

3. Daisy-chain Input active or open: (DSY CHN)flashing red LED
4. +12V Fail: (12V) flashing red LED

5. Alarm: ALM flashing red LED
   Indicates that the system is tripped and the I&A outputs are open.

6. Lock jumper in: LOCK amber LED
   Indicates that the jumper which inhibits the setting of the inhibits is in place.

7. Test jumper in: TEST amber LED
   Indicates that the jumper which inhibits the VME testing of the module is in place.

B. Front panel controls

1. Select Inhibit push-button switch
   Pushing this switch enables the individual channel's Reset/Inhibit switches to set or reset the inhibit when pressed.

2. Reset/Inhibit push-button switches
   Individual channel push-button switches used to reset a trip state and set or reset the inhibit when the Select Inhibit switch is pushed. When pressed by itself the trip state on that particular channel will be reset if the error causing the fault has been cleared. When pressed simultaneously with the Select Inhibit switch it will set or reset the inhibit for that channel. However the inhibit can only be set if the Lock Inhibit jumper on the printed-circuit board is removed.

3. Trip test push-button switch
   Used to check the Daisy-chain, Alarm and Interlock output signals. The system will be in alarm mode as long as this switch is pushed, the alarm LED will flash.

C. Connectors

Error inputs, I&A-1 and I&A-2 outputs on the VMEbus P2 connector.
Daisy-chain In and Daisy-Chain Out (CHAIN IN/OUT) LEMO connectors.

V. Input and Outputs

VMEbus P2 connector (pinout to be determined)

Pin Number	Row A	Row C
1	Channel 0 Input +	Channel 0 Input -
2	Channel 1 Input +	Channel 1 Input -
3	Channel 2 Input +	Channel 2 Input -
4	Channel 3 Input +	Channel 3 Input -
5	Channel 4 Input +	Channel 4 Input -
6	Channel 5 Input +	Channel 5 Input -
7	Channel 6 Input +	Channel 6 Input -
8	Channel 7 Input +	Channel 7 Input -
9	I&A-1 Output +	I&A-1 Output -
10	I&A-2 Output +	I&A-2 Output -

VI. Personality Module

The Personality Module is a daughterboard that plugs onto the VME SIAM board.
It performs the following functions:

1. Jumper selection to determine whether interlock voltage is supplied by the VME module or by an external source.
2. Jumper selection to determine true-high or true-low logic for the interlock input state
3. Jumper selection of the Personality Module I.D.
4. Establish the first VME SIAM module in the daisy chain.
5. Integration Time (R-C time constant selection) is selected by the choice of resistor values. An input fault condition must last for at least a period of time determined by the R-C time constant in order to cause an alarm.

A. Connector
SAMTEC Part No. BST-122-09-T-D-230-RA

1. Pin Assignment

Function	**Ch No.1**	**Ch No.2**	**Ch No.3**	**Ch No.4**	**Ch No.5**	**Ch No.6**	**Ch No.7**	**Ch No.8**
Integration time Rx, Pin No.	1	2	3	4	5	6	7	8
Input polarity select, Pin No.	9	10	11	12	13	14	15	16
Ground for contact input, Pin No.	17	19	21	23	25	27	29	31
12V for contact input, Pin No.	18	20	22	24	26	28	30	32
Module ID bit	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Pin No.	38	40	42	44	37	39	41	43
Ground Pin	33							
Start of Daisy chain Pin (Gnd)	34							
+5V	35							
+12V Pin	36							

2. Integration time set by resistors R9 through R16 for channels 1 through 8 respectively (Subject to change):

Resistor	100 Ω	3.3 kΩ	12k Ω	22k Ω	200 kΩ	1 MΩ	2.2 MΩ	4.7 MΩ	5.6 MΩ	10 MΩ	15 MΩ	18 MΩ	22 MΩ
Time delay	250 µs	10 ms	50 ms	100 ms	1 s	5 s	10 s	20 s	25 s	43 s	66 s	80 s	105 s

3. Integration time variation vs. temperature for e.g. 22MΩ resistor (subject to change)

Temperature in ^{o}C	-7.16	25	57	75
Delay in seconds	105	105	111	116

4. Configuration for selection of external voltages or switch contacts

Channel	+12V jumper	Ground jumper	Polarity jumper	Integration time
1	JP1	JP9	JP17	R9
2	JP2	JP10	JP18	R10
3	JP3	JP11	JP19	R11
4	JP4	JP12	JP20	R12
5	JP5	JP13	JP21	R13
6	JP6	JP14	JP22	R14
7	JP7	JP15	JP23	R15
8	JP8	JP16	JP24	R16
Daisy chain start		JP25		

B. Sample configuration using channel 1:

I. Contact Input, see Figure 2.
1. Switch input NC, opens for fault condition
   JP1 jumpered
   JP9 jumpered
   JP17 open
2. Switch input NO, closes for fault condition
   JP1 jumpered
   JP9 jumpered
   JP17 jumpered

II. Voltage input, see Figure 3.
1. Voltage input normally 0, goes to 1 for fault condition
   JP1 open
   JP9 open
   JP17 open
2. Voltage input normally 1, goes to 0 for fault condition
   JP1 open
   JP9 open
   JP17 jumpered

C. Daisy chain
1. JP25 jumpered when unit is at the beginning of the daisy chain
2. Connector to be specified

VII. VMEBus summary

A. A24, D32, D16 compatible
Eleven registers as shown below

$XX0000_{16}$	Status Register
$XX0004_{16}$	ID register
$XX0008_{16}$	Channel 0 Inhibit register
$XX000C_{16}$	Channel 1 Inhibit register
$XX0010_{16}$	Channel 2 Inhibit register
$XX0014_{16}$	Channel 3 Inhibit register
$XX0018_{16}$	Channel 4 Inhibit register
$XX001C_{16}$	Channel 5 Inhibit register
$XX0020_{16}$	Channel 6 Inhibit register
$XX0024_{16}$	Channel 7 Inhibit register
$XX0028_{16}$	Inhibit register read
$XX002C_{16}$	Reset register
XX003016	Test register

B. Status Register: (address XX0000$_{16}$)

D32 operation only

All the information presented on the front panel LEDs is available to the VMEbus via the 32 bit Status register as follows:

Bit 0	Channel 0 OK	Set to one when no error is detected.
Bit 1	Channel 0 inhibit	Set to one when the inhibit is set (no alarm).
Bit 2	Channel 0 trip	Set to one when a fault has been detected.
Bit 3	Channel 1 OK	
Bit 4	Channel 1 inhibit	
Bit 5	Channel 1 trip	
Bit 6	Channel 2 OK	
Bit 7	Channel 2 inhibit	
Bit 8	Channel 2 trip	
Bit 9	Channel 3 OK	
Bit 10	Channel 3 inhibit	
Bit 11	Channel 3 trip	
Bit 12	Channel 4 OK	
Bit 13	Channel 4 inhibit	
Bit 14	Channel 4 trip	
Bit 15	Channel 5 OK	
Bit 16	Channel 5 inhibit	
Bit 17	Channel 5 trip	
Bit 18	Channel 6 OK	
Bit 19	Channel 6 inhibit	
Bit 20	Channel 6 trip	
Bit 21	Channel 7 OK	
Bit 22	Channel 7 inhibit	
Bit 23	Channel 7 trip	
Bit 24	VME test	Set to one when bit 0 of the test register has been written with a one.
Bit 25	Alarm	Set to one when the alarm, interlock, and daisy-chain outputs are active.
Bit 26	Daisy-chain active	set to one when daisy-chain is open or driven high from another module.
Bit 27	12 Volt failure	Set to one when 12 Volt fails.
Bit 28	Inhibit Lock	Set to one when the jumper to lock-out the inhibits is loaded.
Bit 29	Inhibit Test	Set to one when the jumper to inhibit the VME test is loaded.
Bit 30	Test switch	Set to one when the front panel test switch is depressed
Bit 31		

C. ID register: (address XX0004$_{16}$)

D16 operation only

Sixteen bit read only register.

Bits 0 through 7 correspond to SIAM ID bits 0 through 7 respectively

Bits 8 through 15 correspond to SIAM Personality Module ID bits 0 through 7 respectively

D. Inhibit registers: (address $XX0008^{16}$-$XX024^{16}$)

D16 operation only

Eight write only registers, bit 0 set to one to set the inhibit for each channel and set to zero to reset the inhibit (the last value written in bit 0 of each register can be read back via the Inhibit read register). The inhibit cannot be set if the inhibit lock-out jumper is in. Address XX0008 is used to control the inhibit for channel 0, address XX0024 is used to control the inhibit for channel 7.

E. Inhibit read register: (address $XX0028^{16}$)

D16 operation only

Sixteen bit read only register.

Bits 0 through 7 indicate what is the last value written in bit 0 of the Inhibit registers XX0004 through XX000E respectively. These bits do not reflect the state of the channels inhibit, the state of the inhibit can only be read via the status register. Bits 8 through 15 are zero.

F. Reset register: (address $XX002C^{16}$)

D16 operation only

Sixteen bit register, Writing a one in bits 0 through 7 reset a trip state in channels 0 through 7 respectively. Writing a zero in any bit does not effect any function of the SIAM.

When reading back bits 0 through 7 indicate the last reset operation performed, they do not reflect the channels trip state. Bits 8 through 15 are zero.

G. Test register: (address XX003016)

D16 operation only

Writing a one to bit zero causes the daisy-chain output, and the I&A output transistor to open if the VME Test Disable jumper is not installed.

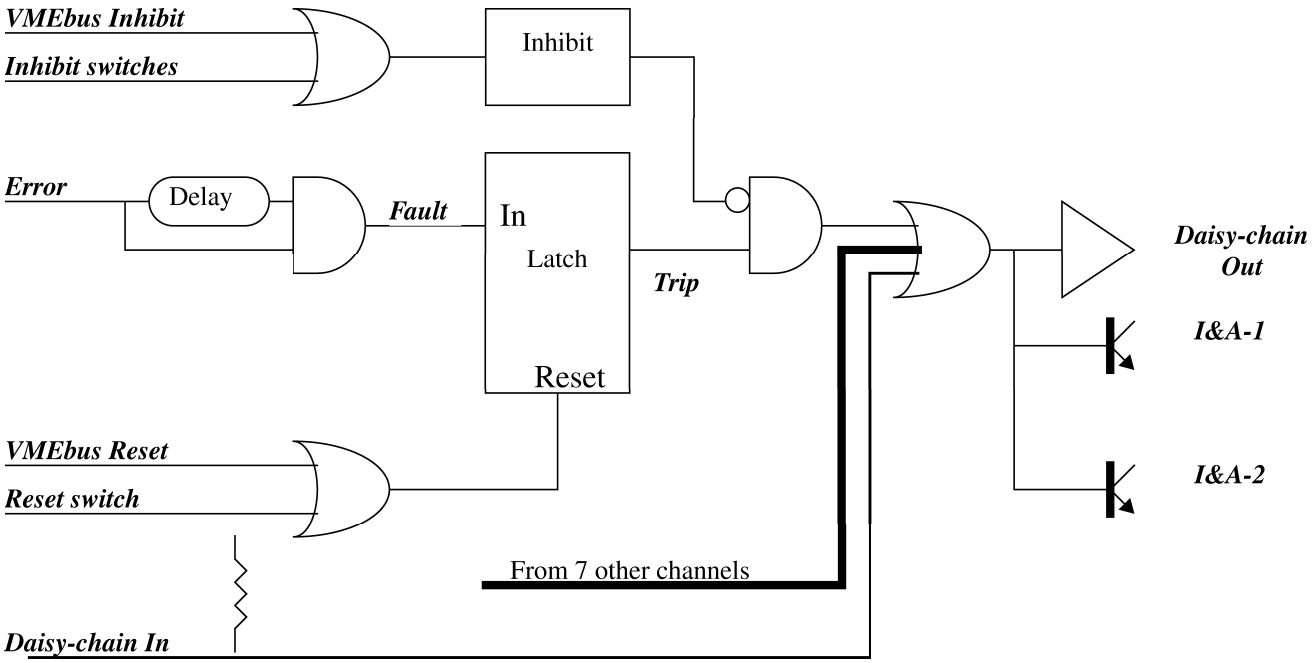

Figure 1. Block diagram of one SIAM channel (optical isolation not shown)

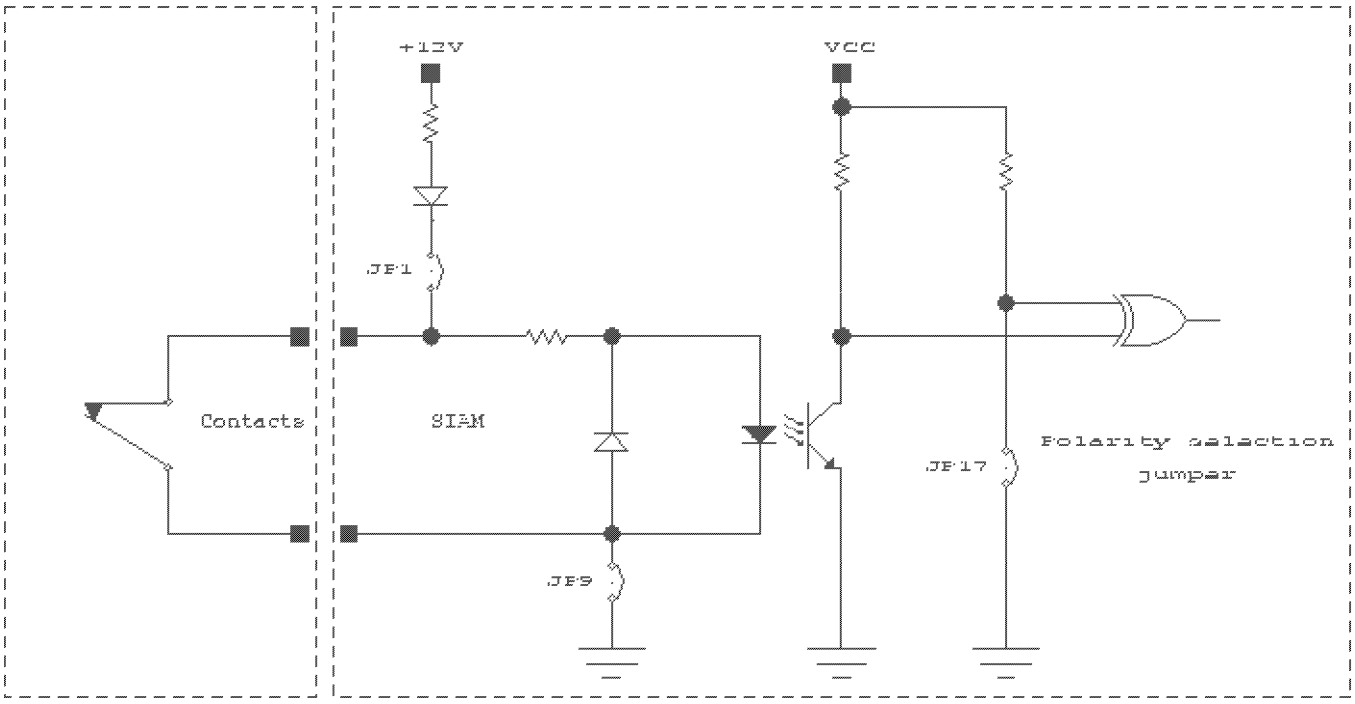

Figure 2. Contact input configuration
(Jumpers shown for channel 1, JP17 open for NC contact)

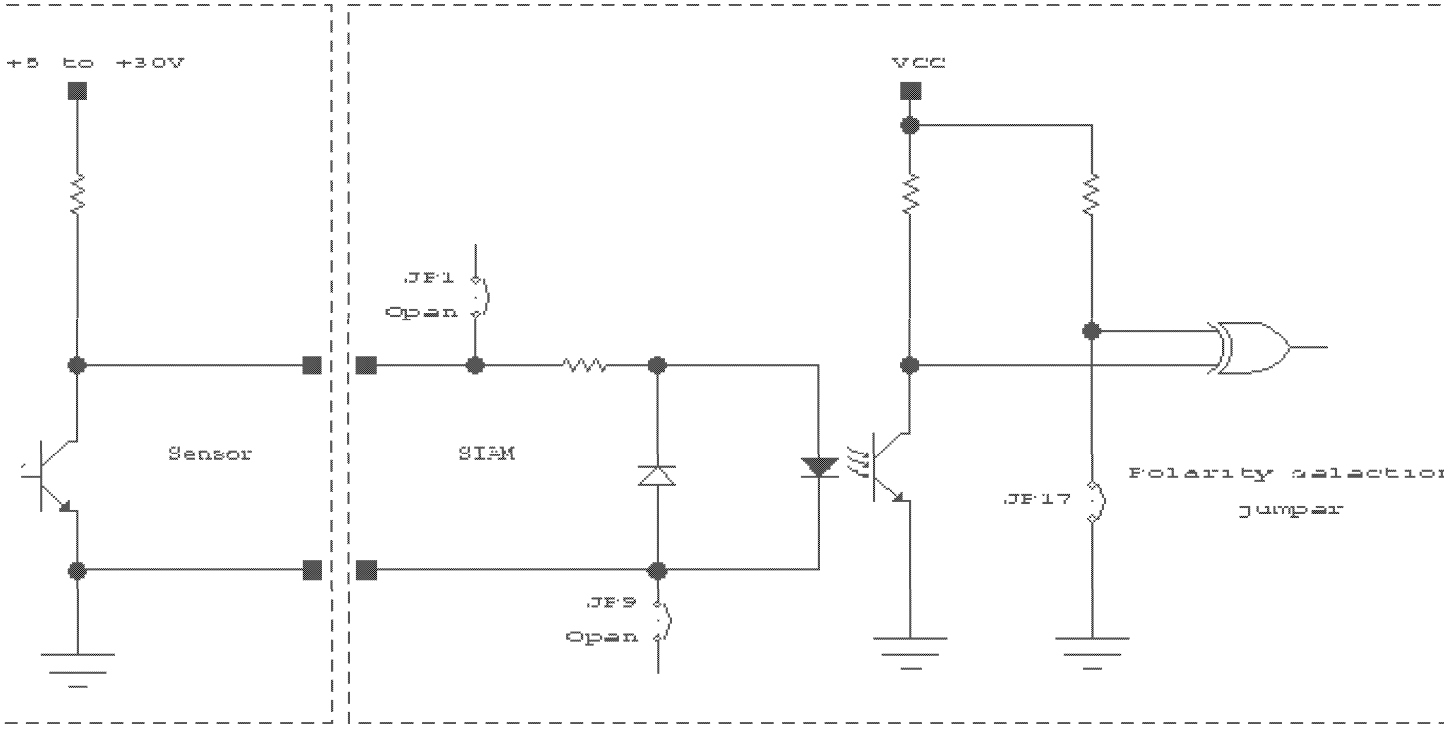

Figure 3. Opto-isolated voltage input configuration

(Jumpers shown for channel 1, JP17 open for active high logic)

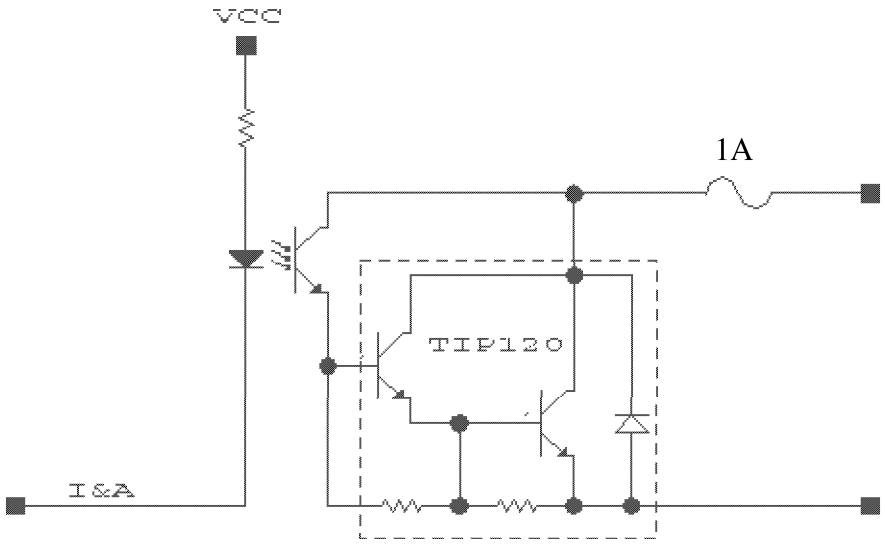

Figure 4. Opto-isolated output (one of two)

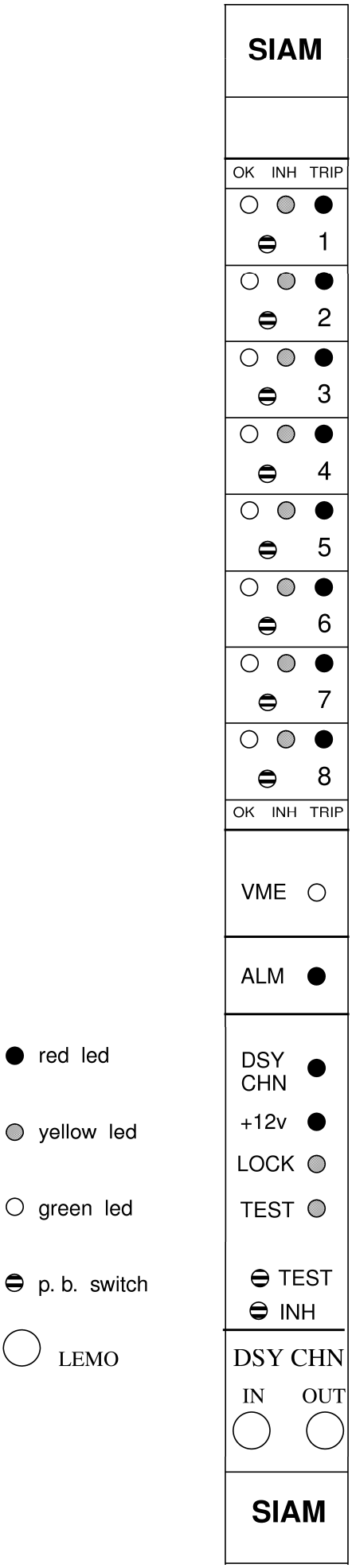

Figure 5. SIAM Front Panel
(subject to change)

VME SUMMARY INTERLOCK AND ALARM MODULE
VME SIAM

I. Description:

The Summary Interlock and Alarm Module (SIAM)[1] is a VMEbus compatible module which can generate an output signal (trip) based on the latched state of eight input conditions (faults). Several modules can be daisy-chained to form a larger set of input conditions. In its simplest form this is an expandable eight input OR gate.
A block diagram of one SIAM channel is shown in Figure 1.
The module has eight optically isolated inputs which may be connected to sensors or relays which detect error conditions. If an ***error*** lasts longer than a predetermined time it causes a ***fault*** condition which is latched. An ***inhibit***, programmable from either the front panel or the VMEBus, is associated with each input. This inhibit can be set to prevent any channel's fault from generating a ***trip*** state. A jumper selectable option disables this feature to prevent inadvertent inhibit of critical subsystems. A trip state drives the module's Interlock and Alarm (I&A) optically isolated outputs, and the daisy-chain output. A latched fault can be reset from either the front panel or the VMEbus only when the error signal itself has disappeared.
A personality module (mezzanine board) provides programmability via jumpers and resistors to configure each input independently. An input can be connected to either normally open or normally closed contacts (Figure 2), or it can be optically isolated to accept an active high or an active low logic signal (Figure 3). A time constant determines how long an input error signal condition must be present before it causes a fault.
Two optically isolated outputs (Figure 4) labeled I&A-1 and I&A-2 are used to indicate an uninhibited fault condition within the module or within a module located upstream in a chain of modules. For example, one output could be connected to an interlock system and the other one to an alarm system.
The expansion ability to accommodate more than eight inputs is provided by the Daisy-chain input and the Daisy chain output. The Daisy-chain input is TTL compatible, and the Daisy-chain output is a TTL open collector output.
Indicators and a status register are provided for visual and computer monitoring of the module.

II. Mode of operation

Since the bits in the status register duplicate the information presented via front panel LEDs, we will refer only to the LED's status within this section, a lit or flashing LED correspond to a bit set to one in the status register.
The first step in using the SIAM consists of determining what conditions may generate an interlock and/or an alarm for the system being monitored. If eight or less conditions are enough only one module is required. If however, there are more than eight error conditions two or more modules will need to be daisy-chained. A single SIAM system or the first module in a multiple SIAM system must have either its daisy-chain input pulled down to ground, or the Start of Daisy chain

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pin, on the personality module, tied to ground. In a multiple SIAM system the daisy-chain output of the first module is connected to the daisy-chain input of the following module and so forth, the interlock and alarm are, in general, generated by the last module in the chain (the SIAM which detects a fault and all SIAMs located after it in the daisy-chain have their I&A output transistors non conducting (open)).

Next, for each type of sensor the corresponding input needs to be configured for:

- Contact closure or contact break if the module provides the voltage to the sensor
- Active high or active low logic level signal if the voltage is supplied by the sensor (the input is then optically isolated).
- The minimum duration the error condition must be present to generate a trip signal

This is done with resistor selection and jumpers on the personality module as explained in section VI.

In the following example we look at only one module, but a chain of modules will function in a similar manner, the inputs of the first module in the chain look like the inputs of a single module system and the outputs of the last module look like the outputs of a single module system.

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When permitted (lock inhibit jumper removed) any channel trip can be inhibited so that it does not generate a system trip condition, thus not changing the state of the daisy-chain, I&A-1, and I&A-2 outputs. This operation is done by either, depressing simultaneously the ***Select Inhibit*** switch and the channel's Reset/Inhibit switch or writing a one in bit 0 of the channel's inhibit register. When a channel is inhibited its functionality is not altered but it will not change the module's Daisy-chain and I&A output signals if an error is detected. This inhibit can be cleared by either, depressing simultaneously the Select Inhibit and the channel's Reset/Inhibit switches or writing a zero in bit 0 of that channel's inhibit register. When the inhibit is set the Inhibit LED for that inhibited channel flashes on and off.

The module can be tested manually or via VME. In the manual mode depressing the Test push-button switch will always cause the Daisy-chain output, and the I&A output transistors to open as long as the switch is depressed. In the programmable mode writing a one to bit 0 of the test register will have the same effect as depressing the Test switch, writing a zero in bit zero of the test register will have the same effect as releasing the Test switch. However, this VME test feature is disabled when the VME Test Disable jumper is installed.

III. Module Specifications:

A. Module type: Single width VME module

B. Input channels: Eight

C. Input levels:

1. User supplied external voltages
   "0" = -30V to +1V
   "1" = +3V to +30V
   Undefined from +1V to +3V
   Input optically isolated with current drawn not to exceed 15 mA at 30V
2. User supplied contacts
   Normally open (NO)
   Normally closed (NC)
3. Daisy-chain In
   TTL with 5kΩ pull-up to +5V

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1. Two identical Alarm and Interlock (I&A-1 and I&A-2): Optically isolated power transistor, TIP120, NPN darlington
   Emitter and collector available as a switch; closed when there is no fault, open when there is an uninhibited trip.
   Ratings:
   Maximum collector voltage: 35V
   Maximum current: 0.5A, collector fused at 1A
   Built-in base emitter shunt resistors and output diode
   At 0.5A collector current, transistor voltage, Vce, is 0.5V
   At 1.0A collector current, transistor voltage, Vce, is 0.7V

2. Daisy chain: TTL Open collector active high signal

E. Latching

Each channel independent of other channels

F. Power required

+5V
+12V
If the +12V line fails, a fault condition occurs

G. Protection

Input withstand +/-30V indefinitely; +/-100V for 30 seconds

IV. Front Panel

A. Front panel indicators

1. VME access green LED
2. For each channel:
   OK green LED
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   When a trip indication is latched the red trip LED will continue to flash on and off even though the fault condition that gave rise to the trip may have cleared.If the fault condition clears, the green OK and the blinking red trip LEDs will both be on. To clear the flashing red LED, the Reset/Inhibit switch for that channel must be pushed, or the corresponding bit in the Reset register set (section VII)

3. Daisy-chain Input active or open: (DSY CHN)flashing red LED
4. +12V Fail: (12V) flashing red LED

5. Alarm: ALM flashing red LED
   Indicates that the system is tripped and the I&A outputs are open.

6. Lock jumper in: LOCK amber LED
   Indicates that the jumper which inhibits the setting of the inhibits is in place.

7. Test jumper in: TEST amber LED
   Indicates that the jumper which inhibits the VME testing of the module is in place.

B. Front panel controls

1. Select Inhibit push-button switch
   Pushing this switch enables the individual channel's Reset/Inhibit switches to set or reset the inhibit when pressed.

2. Reset/Inhibit push-button switches
   Individual channel push-button switches used to reset a trip state and set or reset the inhibit when the Select Inhibit switch is pushed. When pressed by itself the trip state on that particular channel will be reset if the error causing the fault has been cleared. When pressed simultaneously with the Select Inhibit switch it will set or reset the inhibit for that channel. However the inhibit can only be set if the Lock Inhibit jumper on the printed-circuit board is removed.

3. Trip test push-button switch
   Used to check the Daisy-chain, Alarm and Interlock output signals. The system will be in alarm mode as long as this switch is pushed, the alarm LED will flash.

C. Connectors

Error inputs, I&A-1 and I&A-2 outputs on the VMEbus P2 connector.
Daisy-chain In and Daisy-Chain Out (CHAIN IN/OUT) LEMO connectors.

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3. Jumper selection of the Personality Module I.D.
4. Establish the first VME SIAM module in the daisy chain.
5. Integration Time (R-C time constant selection) is selected by the choice of resistor values. An input fault condition must last for at least a period of time determined by the R-C time constant in order to cause an alarm.

A. Connector
SAMTEC Part No. BST-122-09-T-D-230-RA

1. Pin Assignment

Function	**Ch No.1**	**Ch No.2**	**Ch No.3**	**Ch No.4**	**Ch No.5**	**Ch No.6**	**Ch No.7**	**Ch No.8**
Integration time Rx, Pin No.	1	2	3	4	5	6	7	8
Input polarity select, Pin No.	9	10	11	12	13	14	15	16
Ground for contact input, Pin No.	17	19	21	23	25	27	29	31
12V for contact input, Pin No.	18	20	22	24	26	28	30	32
Module ID bit	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Pin No.	38	40	42	44	37	39	41	43
Ground Pin	33							
Start of Daisy chain Pin (Gnd)	34							
+5V	35							
+12V Pin	36							

2. Integration time set by resistors R9 through R16 for channels 1 through 8 respectively (Subject to change):

Resistor	100 Ω	3.3 kΩ	12k Ω	22k Ω	200 kΩ	1 MΩ	2.2 MΩ	4.7 MΩ	5.6 MΩ	10 MΩ	15 MΩ	18 MΩ	22 MΩ
Time delay	250 µs	10 ms	50 ms	100 ms	1 s	5 s	10 s	20 s	25 s	43 s	66 s	80 s	105 s

3. Integration time variation vs. temperature for e.g. 22MΩ resistor (subject to change)

Temperature in ^{o}C	-7.16	25	57	75
Delay in seconds	105	105	111	116

4. Configuration for selection of external voltages or switch contacts

Channel	+12V jumper	Ground jumper	Polarity jumper	Integration time
1	JP1	JP9	JP17	R9
2	JP2	JP10	JP18	R10
3	JP3	JP11	JP19	R11
4	JP4	JP12	JP20	R12
5	JP5	JP13	JP21	R13
6	JP6	JP14	JP22	R14
7	JP7	JP15	JP23	R15
8	JP8	JP16	JP24	R16
Daisy chain start		JP25		

B. Sample configuration using channel 1:

I. Contact Input, see Figure 2.
1. Switch input NC, opens for fault condition
   JP1 jumpered
   JP9 jumpered
   JP17 open
2. Switch input NO, closes for fault condition
   JP1 jumpered
   JP9 jumpered
   JP17 jumpered

II. Voltage input, see Figure 3.
1. Voltage input normally 0, goes to 1 for fault condition
   JP1 open
   JP9 open
   JP17 open
2. Voltage input normally 1, goes to 0 for fault condition
   JP1 open
   JP9 open
   JP17 jumpered

C. Daisy chain
1. JP25 jumpered when unit is at the beginning of the daisy chain
2. Connector to be specified

VII. VMEBus summary

A. A24, D32, D16 compatible
Eleven registers as shown below

$XX0000_{16}$	Status Register
$XX0004_{16}$	ID register
$XX0008_{16}$	Channel 0 Inhibit register
$XX000C_{16}$	Channel 1 Inhibit register
$XX0010_{16}$	Channel 2 Inhibit register
$XX0014_{16}$	Channel 3 Inhibit register
$XX0018_{16}$	Channel 4 Inhibit register
$XX001C_{16}$	Channel 5 Inhibit register
$XX0020_{16}$	Channel 6 Inhibit register
$XX0024_{16}$	Channel 7 Inhibit register
$XX0028_{16}$	Inhibit register read
$XX002C_{16}$	Reset register
XX003016	Test register

B. Status Register: (address XX0000$_{16}$)

D32 operation only

All the information presented on the front panel LEDs is available to the VMEbus via the 32 bit Status register as follows:

Bit 0	Channel 0 OK	Set to one when no error is detected.
Bit 1	Channel 0 inhibit	Set to one when the inhibit is set (no alarm).
Bit 2	Channel 0 trip	Set to one when a fault has been detected.
Bit 3	Channel 1 OK	
Bit 4	Channel 1 inhibit	
Bit 5	Channel 1 trip	
Bit 6	Channel 2 OK	
Bit 7	Channel 2 inhibit	
Bit 8	Channel 2 trip	
Bit 9	Channel 3 OK	
Bit 10	Channel 3 inhibit	
Bit 11	Channel 3 trip	
Bit 12	Channel 4 OK	
Bit 13	Channel 4 inhibit	
Bit 14	Channel 4 trip	
Bit 15	Channel 5 OK	
Bit 16	Channel 5 inhibit	
Bit 17	Channel 5 trip	
Bit 18	Channel 6 OK	
Bit 19	Channel 6 inhibit	
Bit 20	Channel 6 trip	
Bit 21	Channel 7 OK	
Bit 22	Channel 7 inhibit	
Bit 23	Channel 7 trip	
Bit 24	VME test	Set to one when bit 0 of the test register has been written with a one.
Bit 25	Alarm	Set to one when the alarm, interlock, and daisy-chain outputs are active.
Bit 26	Daisy-chain active	set to one when daisy-chain is open or driven high from another module.
Bit 27	12 Volt failure	Set to one when 12 Volt fails.
Bit 28	Inhibit Lock	Set to one when the jumper to lock-out the inhibits is loaded.
Bit 29	Inhibit Test	Set to one when the jumper to inhibit the VME test is loaded.
Bit 30	Test switch	Set to one when the front panel test switch is depressed
Bit 31		

C. ID register: (address XX0004$_{16}$)

D16 operation only

Sixteen bit read only register.

Bits 0 through 7 correspond to SIAM ID bits 0 through 7 respectively

Bits 8 through 15 correspond to SIAM Personality Module ID bits 0 through 7 respectively

D. Inhibit registers: (address $XX0008^{16}$-$XX024^{16}$)

D16 operation only

Eight write only registers, bit 0 set to one to set the inhibit for each channel and set to zero to reset the inhibit (the last value written in bit 0 of each register can be read back via the Inhibit read register). The inhibit cannot be set if the inhibit lock-out jumper is in. Address XX0008 is used to control the inhibit for channel 0, address XX0024 is used to control the inhibit for channel 7.

E. Inhibit read register: (address $XX0028^{16}$)

D16 operation only

Sixteen bit read only register.

Bits 0 through 7 indicate what is the last value written in bit 0 of the Inhibit registers XX0004 through XX000E respectively. These bits do not reflect the state of the channels inhibit, the state of the inhibit can only be read via the status register. Bits 8 through 15 are zero.

F. Reset register: (address $XX002C^{16}$)

D16 operation only

Sixteen bit register, Writing a one in bits 0 through 7 reset a trip state in channels 0 through 7 respectively. Writing a zero in any bit does not effect any function of the SIAM.

When reading back bits 0 through 7 indicate the last reset operation performed, they do not reflect the channels trip state. Bits 8 through 15 are zero.

G. Test register: (address XX003016)

D16 operation only

Writing a one to bit zero causes the daisy-chain output, and the I&A output transistor to open if the VME Test Disable jumper is not installed.

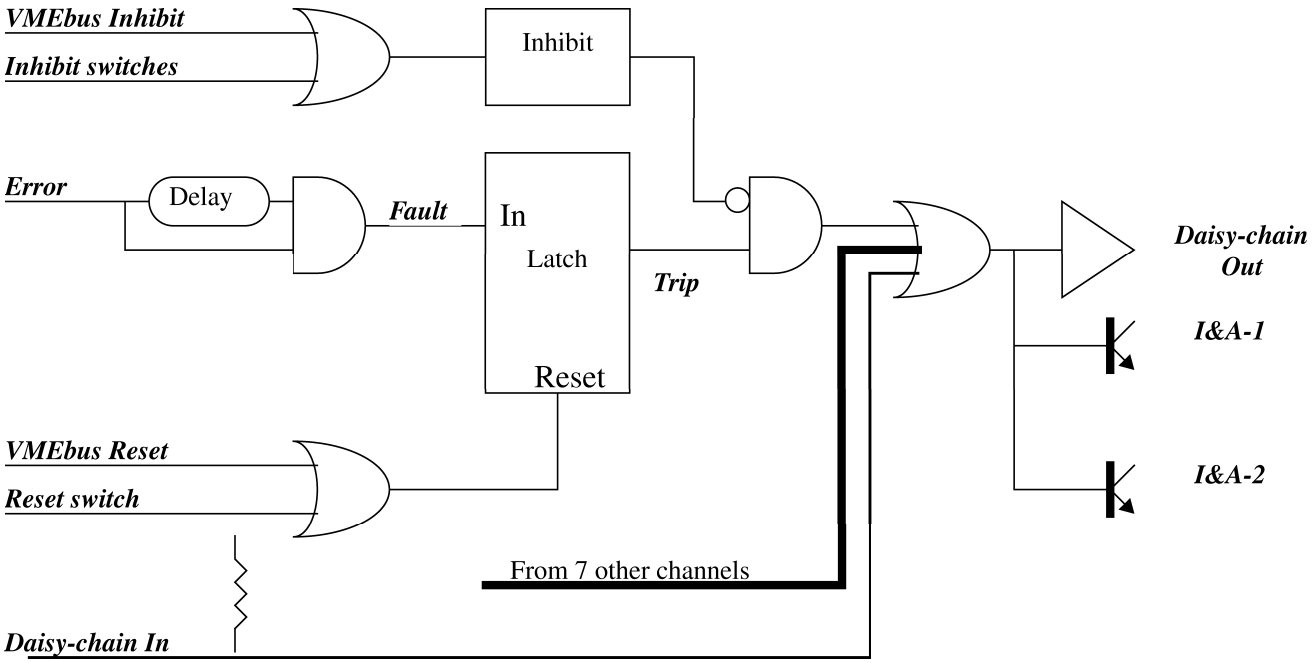

Figure 1. Block diagram of one SIAM channel (optical isolation not shown)

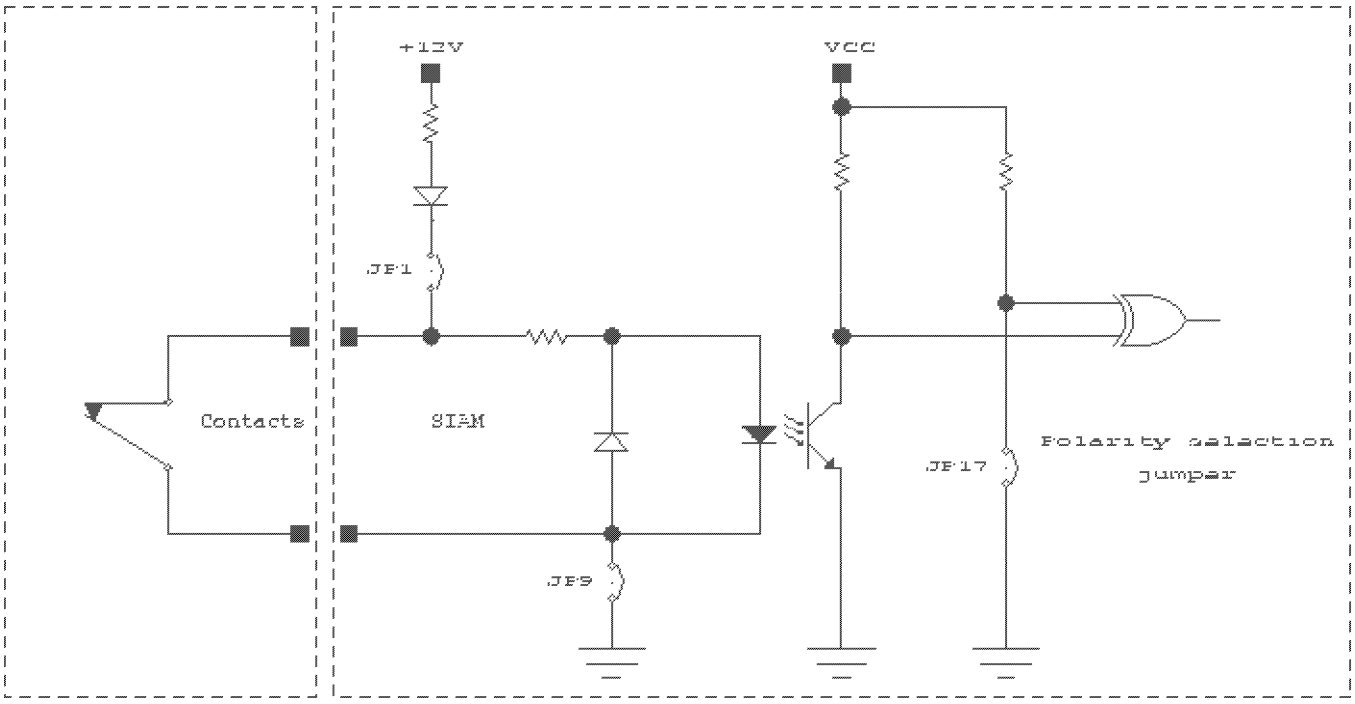

Figure 2. Contact input configuration
(Jumpers shown for channel 1, JP17 open for NC contact)

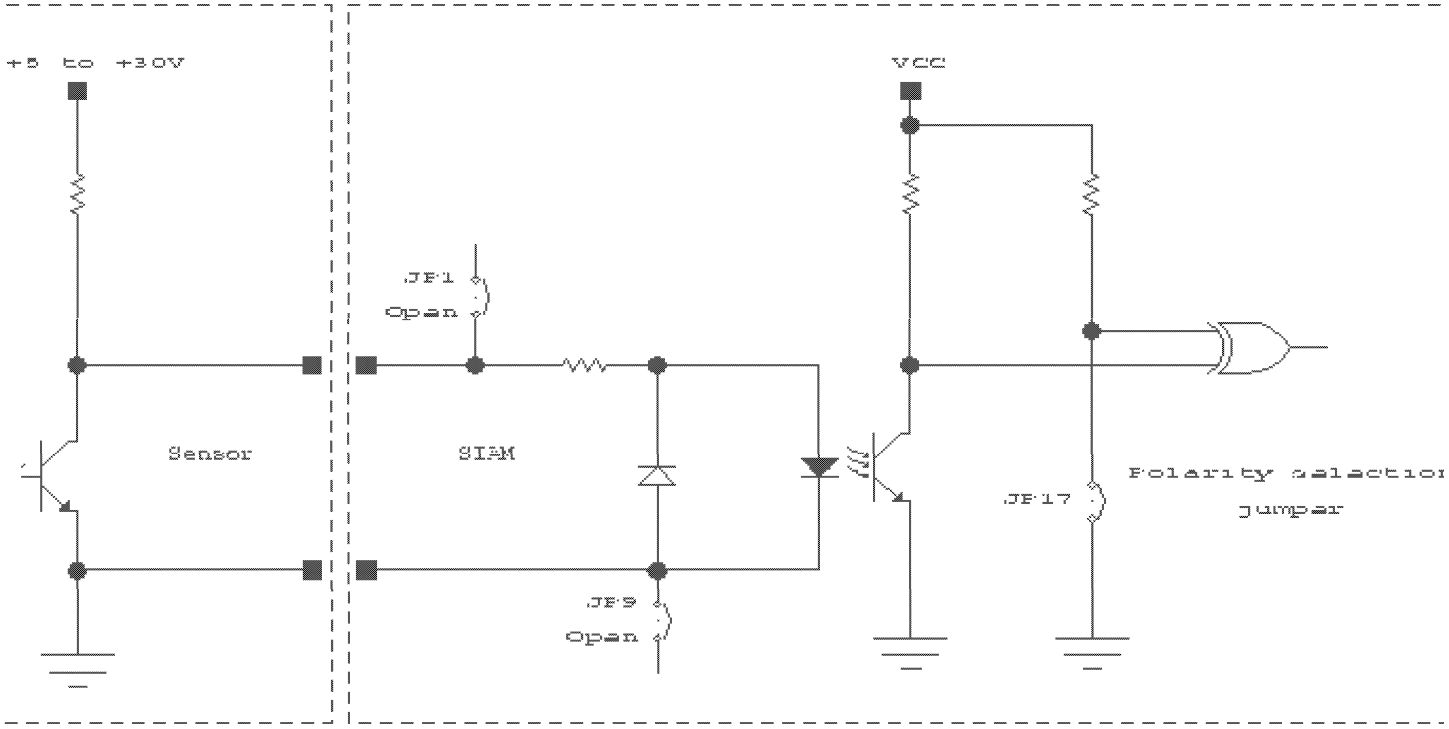

Figure 3. Opto-isolated voltage input configuration

(Jumpers shown for channel 1, JP17 open for active high logic)

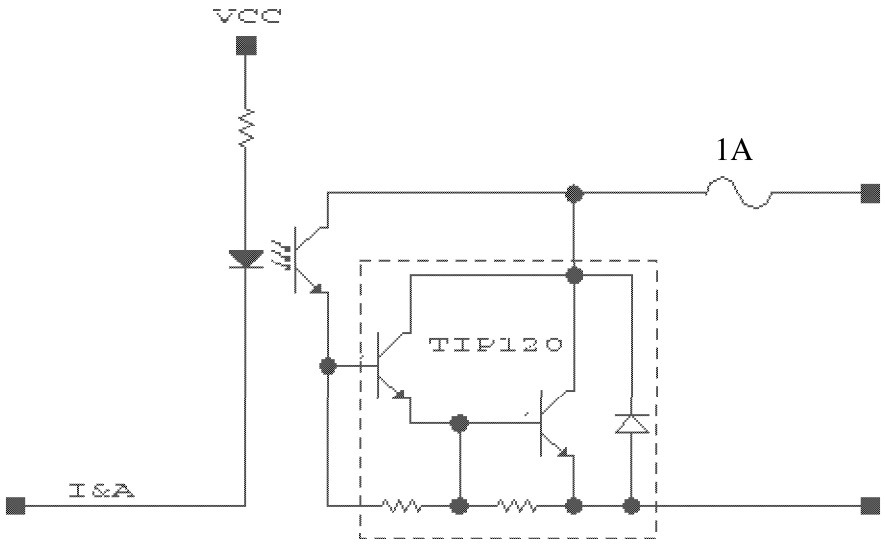

Figure 4. Opto-isolated output (one of two)

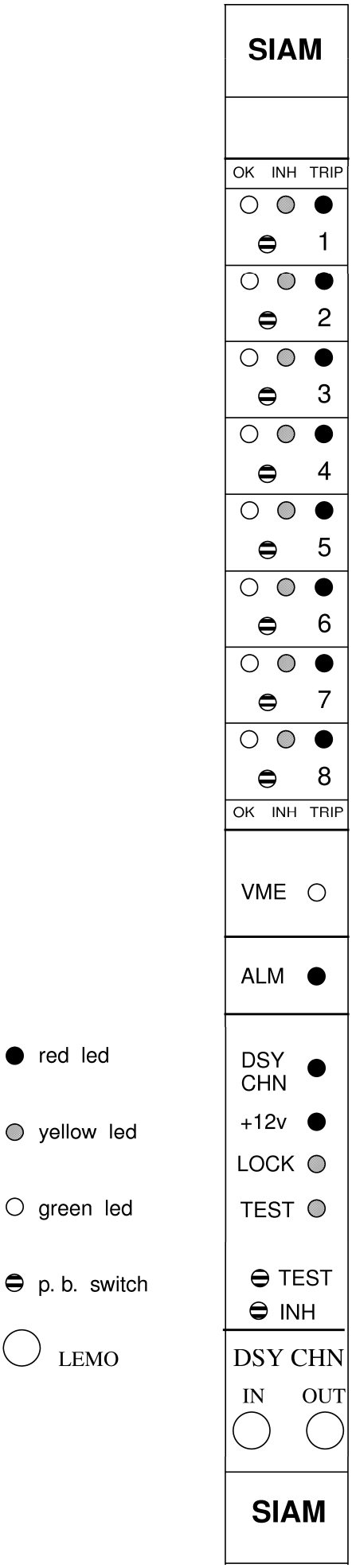

Figure 5. SIAM Front Panel
(subject to change)