Electronics Feasibility Study Using Waveform Digitizers for a 10 ps Time-of-Flight Detector

Mickey Chiu, Sebastian White
Dept of Physics, Brookhaven National Lab

Thomas Tsang
Instrumentation Division, Brookhaven National Lab

William Powell, Richard Dix, Kirk Drummond
Physics Dept, Morgan State University

Cheng-yi Chi
Nevis Labs, Columbia University

September 15, 2010

Abstract

A large acceptance, 10 ps Time-Of-Flight Detector in PHENIX, such as the proposed FOTOF, would require producing over 5000 channels of electronics. The electronics must have resolution of ∼5 ps or better in order to not contribute significantly to the overall timing, and must also have relatively low power draw, as well as being affordable on the scale of thousands of channels. Over the summer of 2010 we studied an approach based on waveform digitizers (HBD and DRS4) and find that we are able to achieve 9 ps for one sample with the DRS4. With two samples one can get $9/\sqrt{2} \sim 6$ ps resolution, and we also achieved better than 2 ps for the full 30 samples on the rising edge. This results proves that an approach based on waveform digitizers should make it possible to build electronics with the required specifications of timing resolution, power load, channel density, and cost for the FOTOF.

1 Introduction

The proposal for a large acceptance 10 ps Time-Of-Flight Detector which will fit within the compact space defined by the current copper nosecone will require, among many other things, demonstration that one can build many thousands of channels of electronics which will have low power draw at the detector connection end, at low enough cost, and contribute less than 5 ps to the overal

timing resolution budget. The low power requirement is to reduce the cooling requirements in the tight space of the inner central part of PHENIX.

In this note we outline studies done over the summer of 2010 which proves that an approach based on waveform digitizers satisfy all of the above requirements. Two different electronics systems are tested, the DRS4 evaluation board from Stefan Ritt of PSI [1, 2], and the HBD ADC electronics from Nevis. The HBD ADC is a 60 MHz ADC based system and is described elsewhere [3].

The DRS4 is an ASIC which implements a radiation hard switched capacitor array (SCA) fabricated in a 0.25 um CMOS process. It is capable of digitizing 9 input channels at up to 6 GSa/s with a depth of 1024 bins and 11.5 bits. It has a high input analog bandwith of 850 MHz, power consumption of less than 40 mW/channel, and a nominal 33 MHz digitization speed which could possibly be extended to 37.5 MHz, or four times the RHIC clock. The typical cost of the chip is $\sim$\$10/channel.

For the next level of timing resolution approaching picosecond resolution, the waveform digitization approach, and in particular the switched capacitor array approach, has several advantages to the standard approaches considered in the past, such as leading edge or constant fraction discriminators with TDC and ADC readout. In these approaches one requires separate readout for the charge and time digitization, and the one threshold with the discriminator limits the possible resolution. Pile-up can become an issue. Also, the standard approaches typically require high power consumption due to the fast ADCs required, not to mention that often a very fast amplifier has to be utilized.

2 Test Setup

To determine the timing resolution of the HBD and DRS4 electronics, we took a signal generated by an Agilent 33250A pulse generator, split it passively with a lemo tee, and fed the two signals into two channels of the electronics. Since the two signals should be identical, up to fluctuations in the charge path which should be very small, the difference in the measurement of the signal gives a measure of the electronics resolution.

A schematic picture of the setup is shown in figure 1, which shows the signal generated in the Agilent, the passive splitter, and then input into the electronics and digitized to the computer for final analysis. For the DRS4 the board is connected directly to the computer by USB. For the HBD, the data is sent through the DCM by fiber and then written to disk via a JSEB.

3 Results

3.1 DRS4 Single Sample Timing Resolution

A picture of the generated signal we used to test the electronics timing resolution is shown in fig 4. The DRS4 provides the waveform at fixed sampling intervals, and in the case of this particular test we ran the DRS4 in the 5 GSa/S mode, or

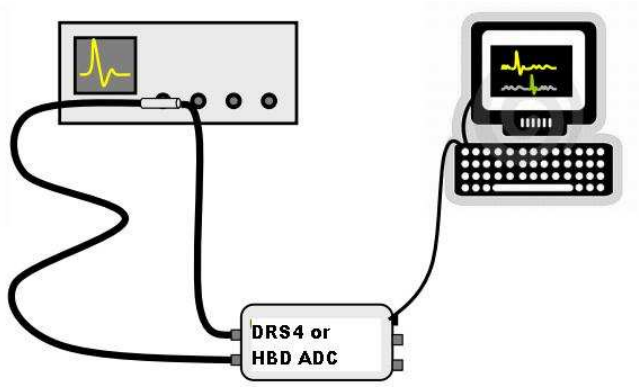

Figure 1: Parametrization of Test Pulse Shape

$\sim$2 ps. The difference in time between the two split signals can be determined from the difference in voltages at a fixed sample point by the relationship

$$\delta t = \frac{\delta V}{m} \tag{1}$$

where m is the slope of the signal at the sampling point, or in other words, m is the risetime. We chose the fastest risetime possible with the Agilent 33250A, 5 ns, with a signal amplitude which nearly saturates the dynamic range of the DRS4, as shown in 2.

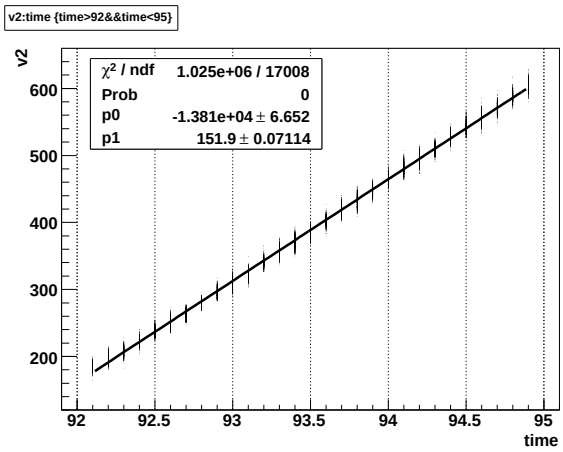

Figure 2: Slope of the rising edge of generated signal.

With a slope of 151.9 mV/ns, and a voltage difference of 1.75 mV RMS, we extract a single sample time resolution for the difference between two signals to be 11.5 ps. The resolution for one signal is then $11.5/\sqrt{2} = 8$ ps.

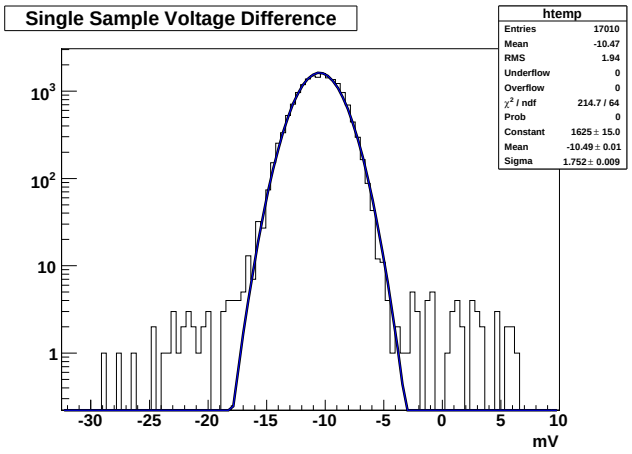

Figure 3: Difference in voltage between the split signals from the DRS4.

3.2 DRS4 Best Timing Using Fit

To find the best possible determination for the time using all of the samples on the rising edge of the generated pulse, we determined a parametrization of the pulse shape using the following functional form:

$$f(t) = \frac{A}{1+e^{\frac{-(t-t_0)}{r}}} + B + C(t-t_0) + D(t-t_0)^2 + E(t-t_0)^3 + F(t-t_0)^4 + G(t-t_0)^5 \tag{2}$$

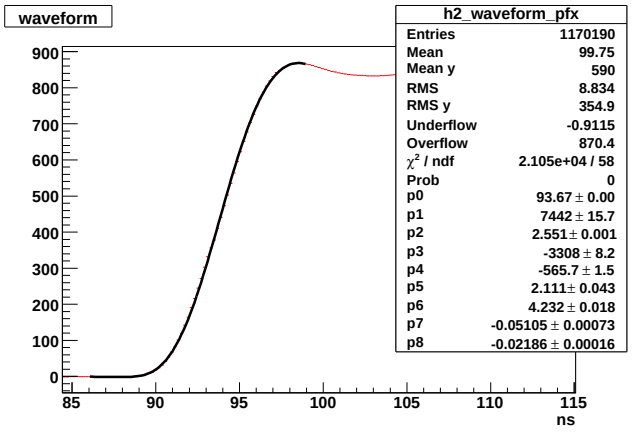

Figure 4: Parametrization of Test Pulse Shape

Figure 4 shows the result of the fit. Using the results of this shape parametrization, we fit the signal for each event to determine the one free parameter, the

start time t_0. The resulting time resolution when using the signal shape is shown in figure 5. The time resolution for the difference between the two pulses is 2.29 ps, which for a single pulse is 1.62 ps. There are about 30 samples on the rising edge, so this is well consistent with the simple scaling from the single sample resolution, ie, $8/sqrt30 = 1.5$ ps.

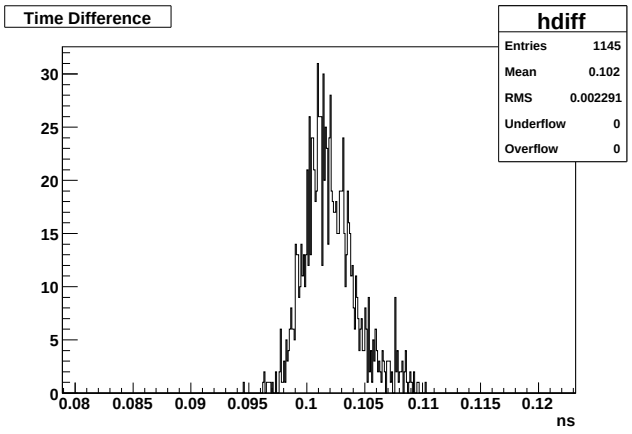

Figure 5: Difference in time using a fit with the parametrized signal shape.

In the case of this pulse from the Agilent generator, the timing resolution is equivalent all along the rising edge of the pulse, as seen in figure 6. Thus the timing resolution should just scale like $1/\sqrt{N_{samples}}$, as we have observed in our study.

For a real pulse from the FOTOF, we expect that the signal timing resolution will be best for the early part of the signal, so a careful study of the resolution differences along the signal will be important.

3.3 HBD ADC Single Sample Timing Resolution

We also investigated the timing resolution of the HBD electronics. In an earlier study for the NCC prototype we had found a resolution of better than 100 ps, but in this earlier study we were limited by the input timing signals and not by the electronics. The very good timing resolution of the HDB ADC was where we first started becoming interested in waveform digitizers for good timing electronics.

We used the same signal as that for the DRS4 study, split into two different HBD channels (ch 174 and 175). Figure 7 shows the difference in the voltage between the two channels for the split signal as a function of the voltage of the signal. There is a large dependence of the mean of the voltage difference depending on where one samples the voltage. However, the rms of the voltage difference is relatively small compared to this variation on the mean. One could possibly go channel by channel and calibrate out these variations in the mean,

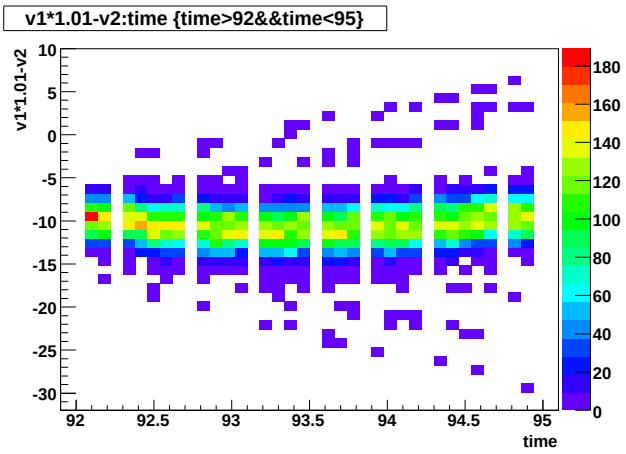

Figure 6: The difference in time as a function of the signal voltage.

which come from different risetimes due to variations in the shaping and input bandwidth for each ADC channel.

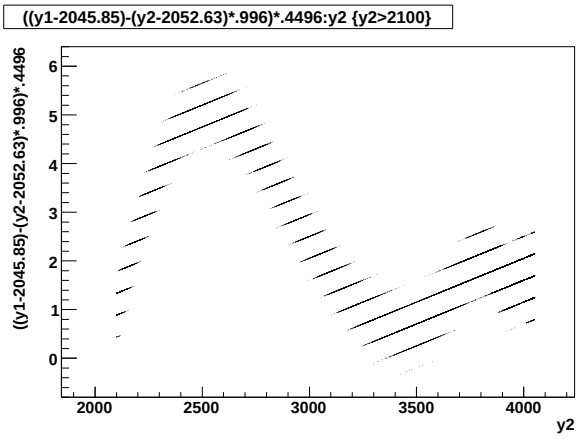

Figure 7: Voltage difference vs ADC (y2) for the split signal into the HBD ADC electronics. The ADC is corrected for the pedestal and scaled to volts.

To get the possible timing resolution of the HBD ADC, we selected a small slice of the signal, using only the part of the signal with amplitudes between 339 and 384 volts. The result is shown in 8. Since the risetime slope at this part of the signal is m $\sim$ 800 mV/30 ns = 26.67 mV/ns, we extract a resolution of $\Delta t = \Delta V/m = 0.34/26.67 = 12.7$ ps, which translates to a resolution of 9 ps for a signal sample.

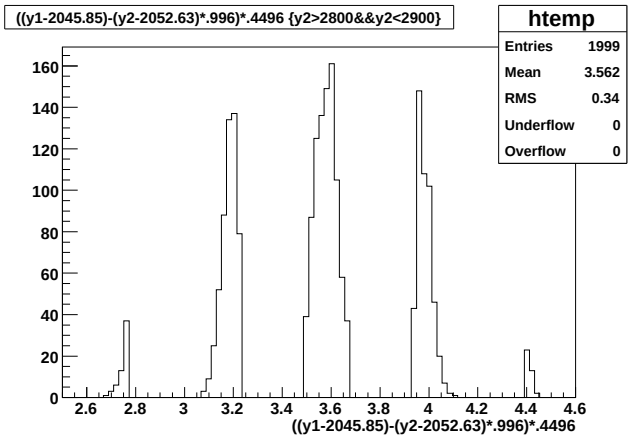

Figure 8: The voltage difference for Voltage between 339 and 384 volts.

4 Conclusion

We have investigated the use of waveform digitizers as the basis for the electronics for a many thousand channel, 10 ps TOF detector such as the FOTOF, and have been able to show as a proof of principle that this approach would successfully satisfy all of the stated requirements. It's even possible that the timing resolution of the DRS4 and HBD ADC are limited by the bandwidth of the input signal, since the Agilent 33250A can only produce 5 ns risetime signals. Testing with very fast detector signals, such as from MCP-PMTs, is under way with cosmics to determine the ultimate timing resolution of the electronics.

Nevertheless, with our crude setup and without optimizing anything, we have achieved 8-9 ps timing resolution from the DRS4, and demonstrated this type of resolution might be possible with the HBD electronics after extended and careful calibration. We also demonstrated that the resolution scales roughly as $1/\sqrt{N_{samples}}$, so that with two samples along the rising edge we can achieve our desired goal of $\sim$5 ps for the electronics contribution.

From this study we also conclude that the fundamental aspects that one wants to control for fast timing is a very fast risetime in the signal and very low signal to noise in the sampling. One can possibly optimize the signal to noise ratio with judicious shaping to keep the fast components of the signal while reducing the noise, as demonstrated in the HBD electronics test. This needs to be studied further, as well as a more realistic implemention of waveform digitization which conforms to the PHENIX DAQ and the specific geometric requirements of the FOTOF.

References

[1] S. Ritt. The DRS chip: Cheap waveform digitizing in the GHz range. *Nucl. Instrum. Meth.*, A518:470–471, 2004.

[2] Stefan Ritt. Design and performance of the 6 ghz waveform digitizing chip drs4. pages 1512 –1515, oct. 2008.

[3] C.-Y. Chi, W. Anderson, B. Azmoun, Z. Citron, A. Dubey, M. Durham, Z. Fraenkel, J. Harder, T. Hemmick, J. Kamin, A. Kozlov, A. Milov, M. Naglis, P. O'Connor, R.P. Pisani, V. Radeka, I. Ravinovich, T. Sakaguchi, D. Sharma, A. Sickles, F.W. Sippach, S. Stoll, I. Tserruya, C. Woody, and B. Yu. A faster digitizer system for the hadron blind detector in phenix. volume 3, pages 1997 –2000, oct. 2007.