Electronics Challenges for HL-LHC pileup Mitigation with HyperFast Timing

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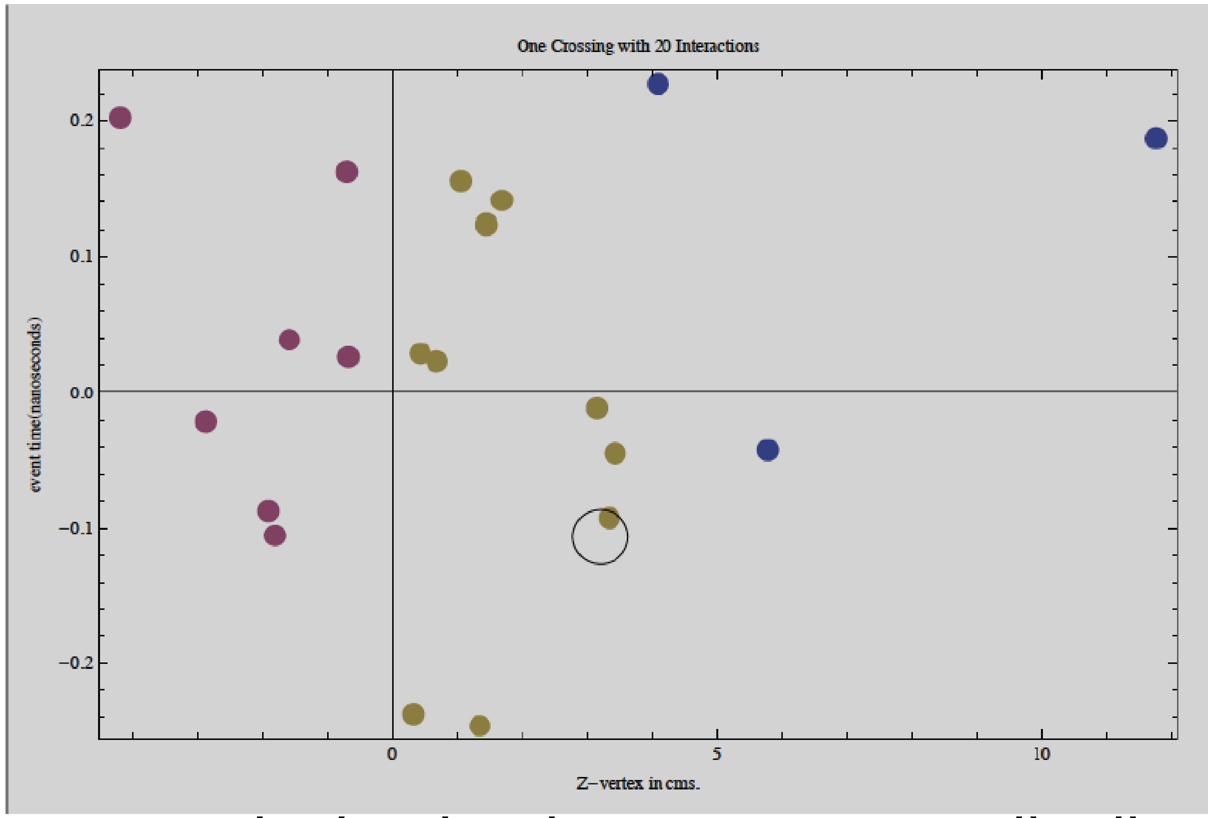
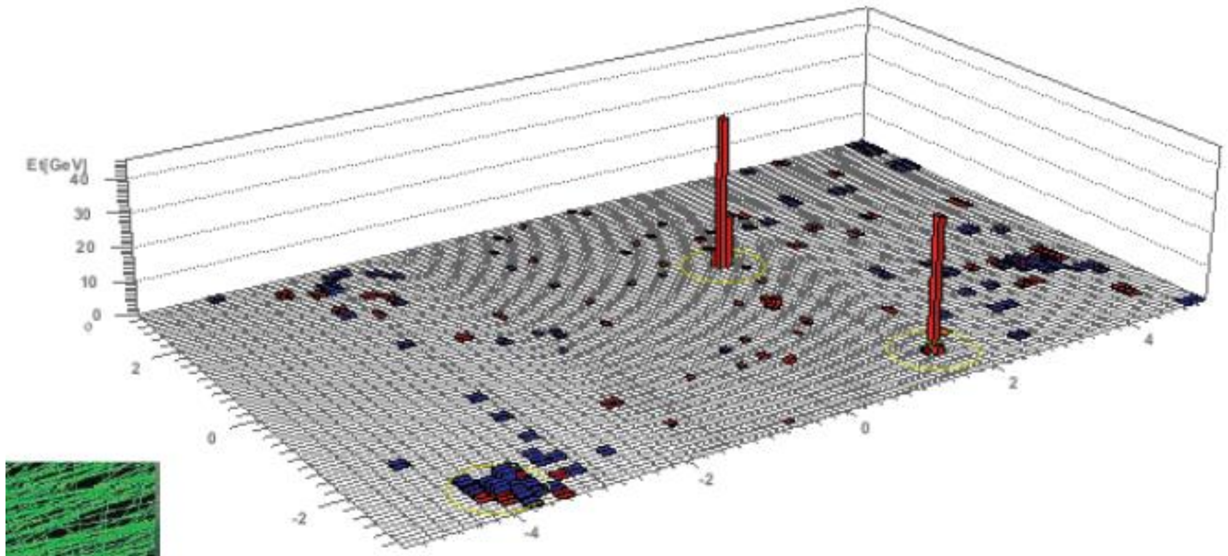
LHC bunch crossing in space and time



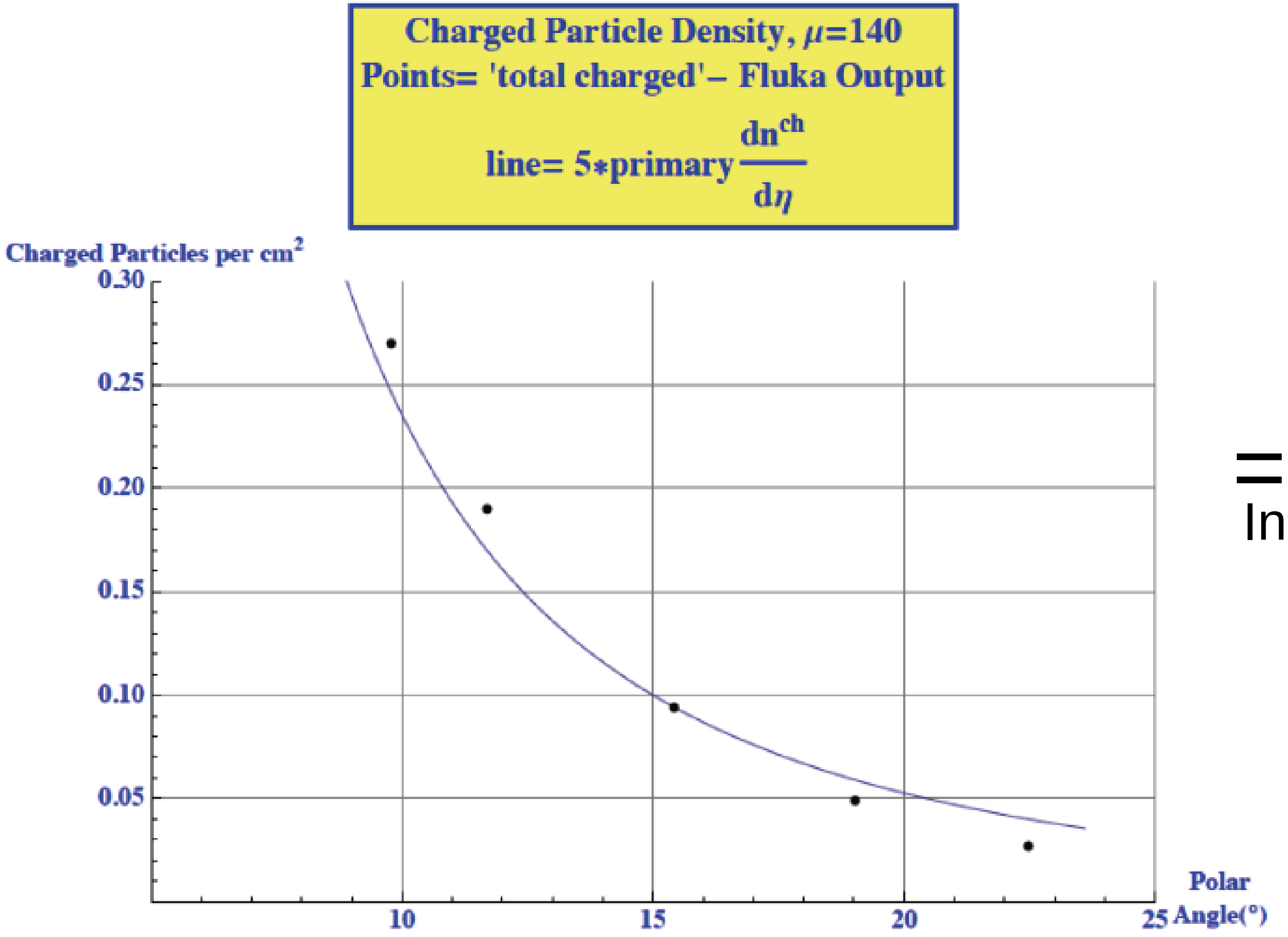


in above Higgs->2 gamma and proton jet fragments observed very forward region

- w. LHC design book parameters z-distribution invariant wrt time and vice versa
- time and z measurement are both potentially tools for pileup mitigation

goal of pileup mitigation in endcap region is to reduce background to eg. VBF jets and MET

Dedicated timing detector layer in current CMS pre-shower volume for TP simulations

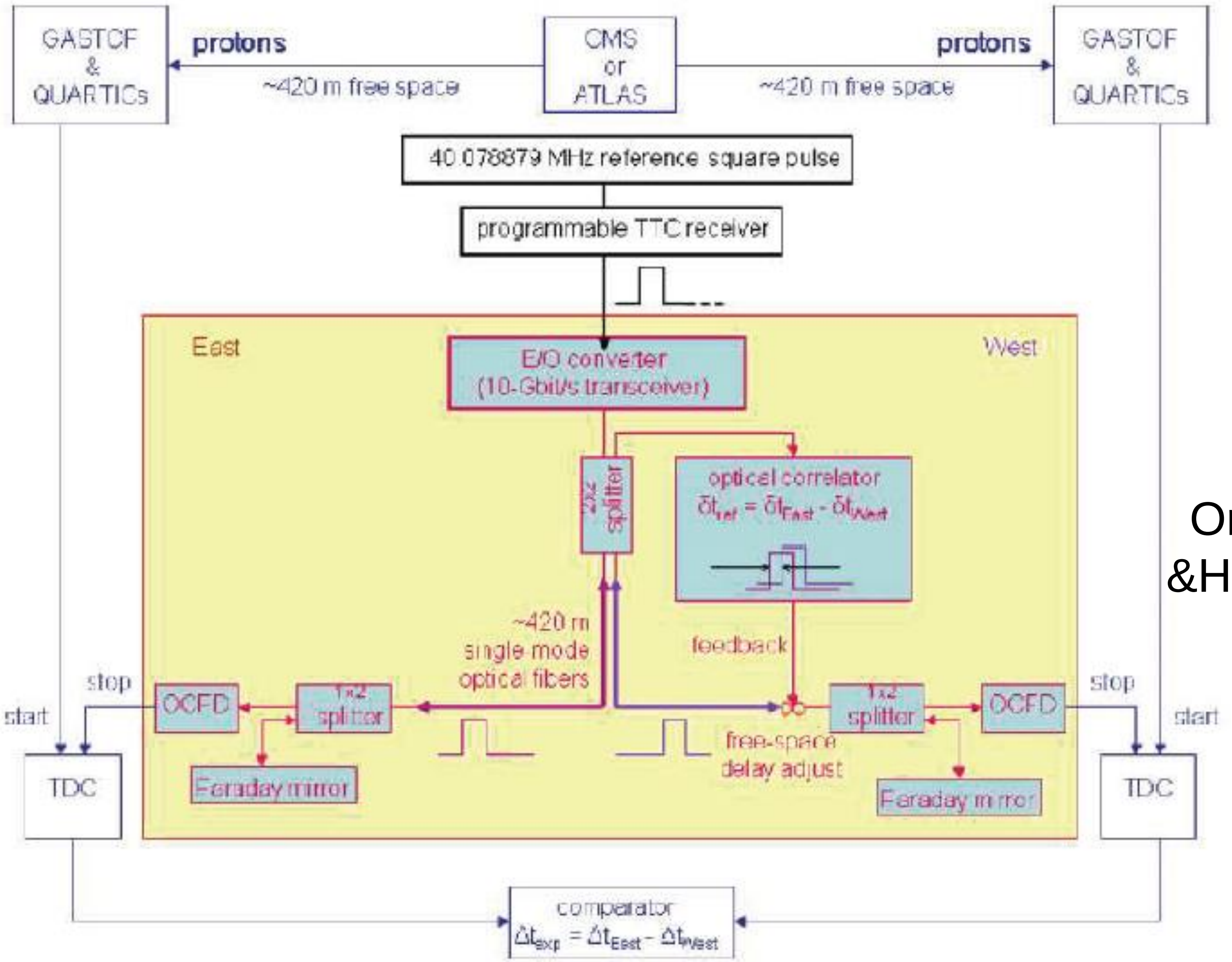


Fluka HL-LHC calculation shows 1 cm**2 is about right pixel size

=> large pixel size Si detector convenient but hard to maintain good signal risetime and response with larger C_{Det}(50-60 pF).

In this presentation discuss fe electronics solution.

Ancilliary systems (ie clock distribution)-we've found cost effective



$60k clock distribution
developed for FP420
(Tsang and SNW-2008)

similarly recent developments
in waveform digitizers at
Orsay/Saclay, PSI, Chicago, Hawaii
&HPTDC ASIC development @CERN
-see Clermont Fd. picosecond
meeting last week

Sensor technology

- previous picosecond timing developments not optimized for 10^{6-7} Hz/cm^2 (eg ALICE TOF, MCP-PMTs, etc)
- solid state sensor SNR an issue (ie CVD diamond)
- conventional Si sensors limited by
  - weighting field uniformity
  - Landau/Vavilov fluctuations
  - SNR

hyperfast Si sensor development

over past several years our collaboration has worked w. RMD/Dynasil on developing a solution to these limitations

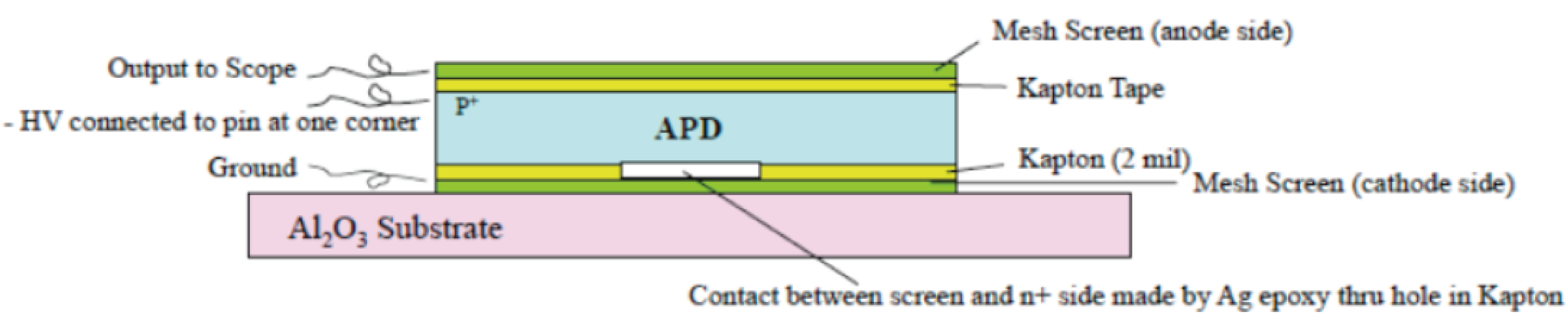
=>Deep Depleted APD/w. Micromegas mesh readout

- Large MiP signal (3600 eh pairs*520 internal APD gain)
- weighting field controlled w. scinterred Au(bottom) and MicroMegas(top) layer
- Landau contribution limited to <9 picosec w. 80% eff’n

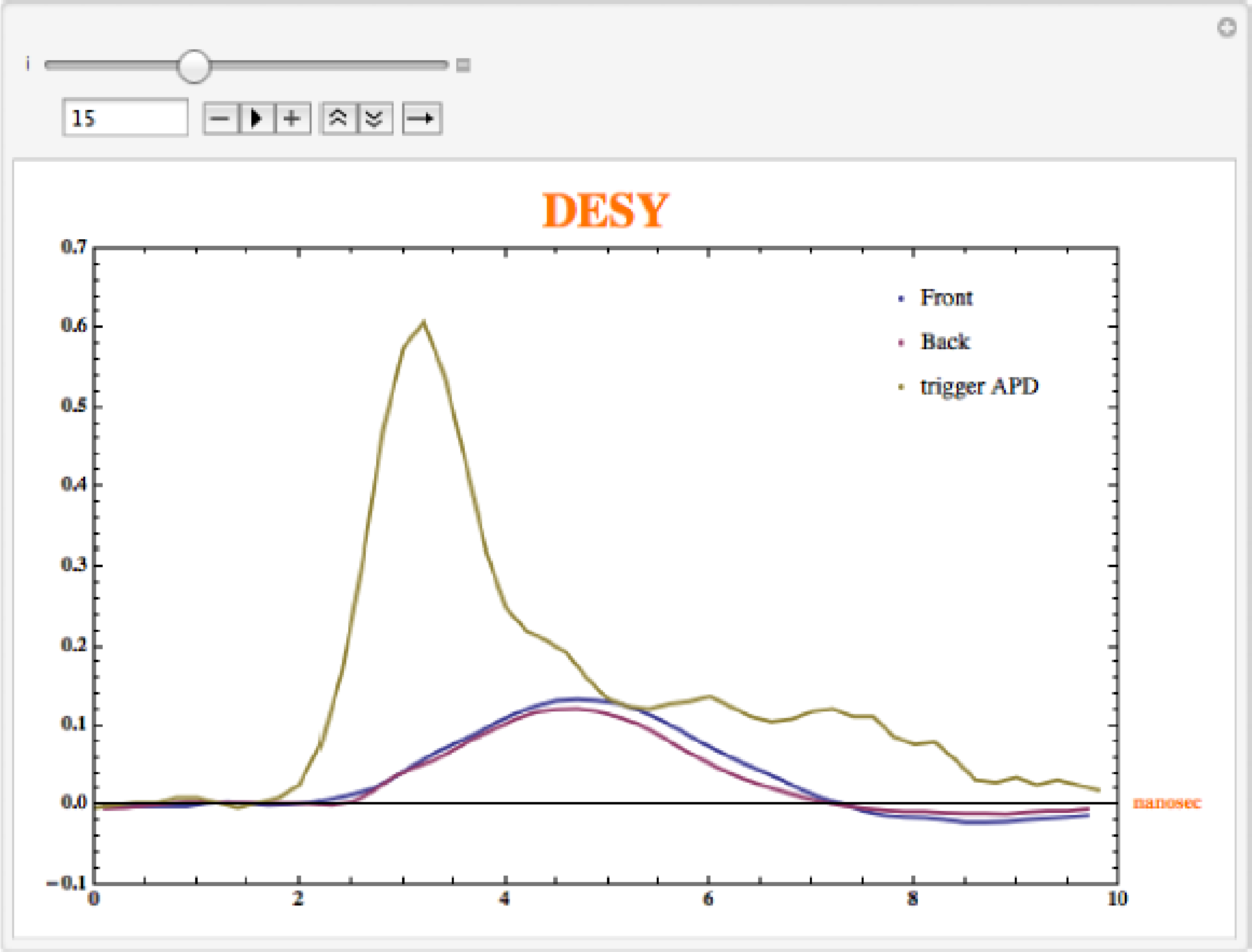
This technology has several other benefits:

- eliminates need for blocking Cap.
- reduces(eliminates?) effect of R_S
- big reduction in time walk and jitter

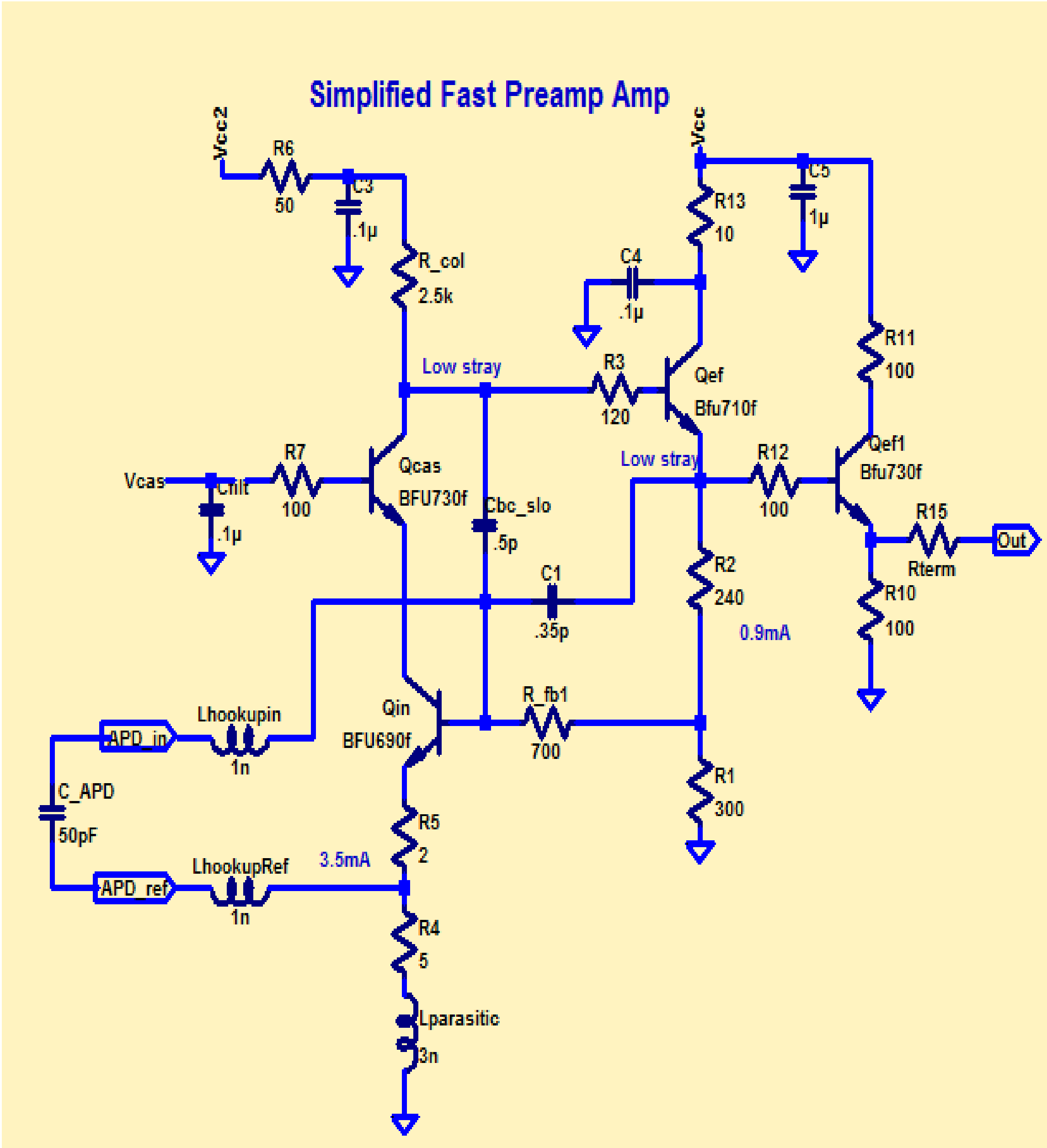
Top Screen Output Connection (capacitively coupled)



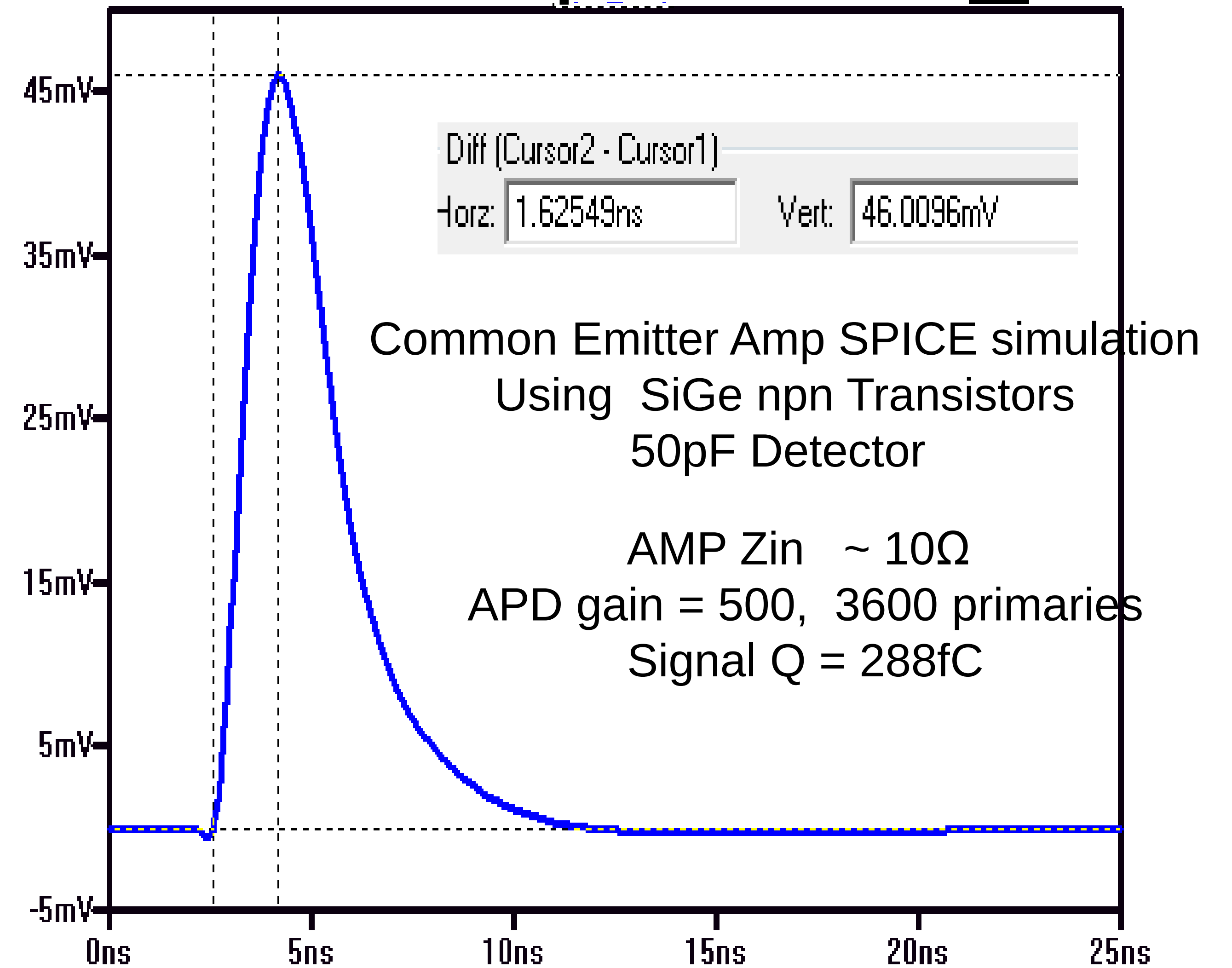
Expected features reproduced in DESY data



Peak amplitude 1/5 that of 4 pF detector
in large area 60 pF detector
and
Risetime degraded from 0.7 to 2 nsec when using 50 ohm voltage amp
We expect significant improvement in Spring PSI run w. new amp.



Preamp Out AC_Vout



APD Preamp Objectives ~1ns Risetime, Low (series) noise,

- **Low RinCTotal Time Const. → Remove as much charge as possible APD Fast APD signal RinCTotal ≈ 1ns → Rin ~ < 20Ω**
- **Limit Amplifier Series Noise Use Low rbb' bipolar Input transistor.**
- **Gain BW ~ >1GHz → Choose Fast Bipolar Transistors**
- **Connections Short, Low inductance → Amplifier within CM of detector**