R&D Targeting CMS preparedness for HL-LHC: pileup mitigation with fast timing

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Purpose

- we propose to build a clear case and assess costs and feasibility for tools to mitigate pileup backgrounds in CMS using picosecond timing.
- this 6 year development has received unique DOE AD R&D award over the years and currently the subject of approved BNL experiment AE-55 (K. McDonald and SNW co-spokespersons)
- the core of the program is the development of Si based solution for ~10 picosecond timing at sustained rates of ~10^7Hz/cm^2 (try to name another solution!!).

- this core activity (7 members from lab/industry/ university) is basis of network now involving 6 additional institutions to address systems aspects of any such timing solution (FEE, digitization, clock distribution...)
- I am charged by Joel Butler to form such a network, extending beyond CMS
- part of strategy has been to form a link with RD52 (dual readout calorimetry) to merge fast timing with their program.
- Aside from weekly meetings with Dynasil, held several meetings at Princeton w. Hamamatsu

- have been meeting with people from Hamamatsu photonics (Japan and NJ) for 6 years on this topic, evaluating their new alternatives to MCP (MCP have, up to now, not been appropriate for LHC rates).

- many discussions about alternative technologies and costs at scale needed for CMS Phase II.

- Hamamatsu has, up to now, been unsuccesful in proposing an alternative to our Si solution