

Fast Timing for Moderate Capacitance APD Amplifiers

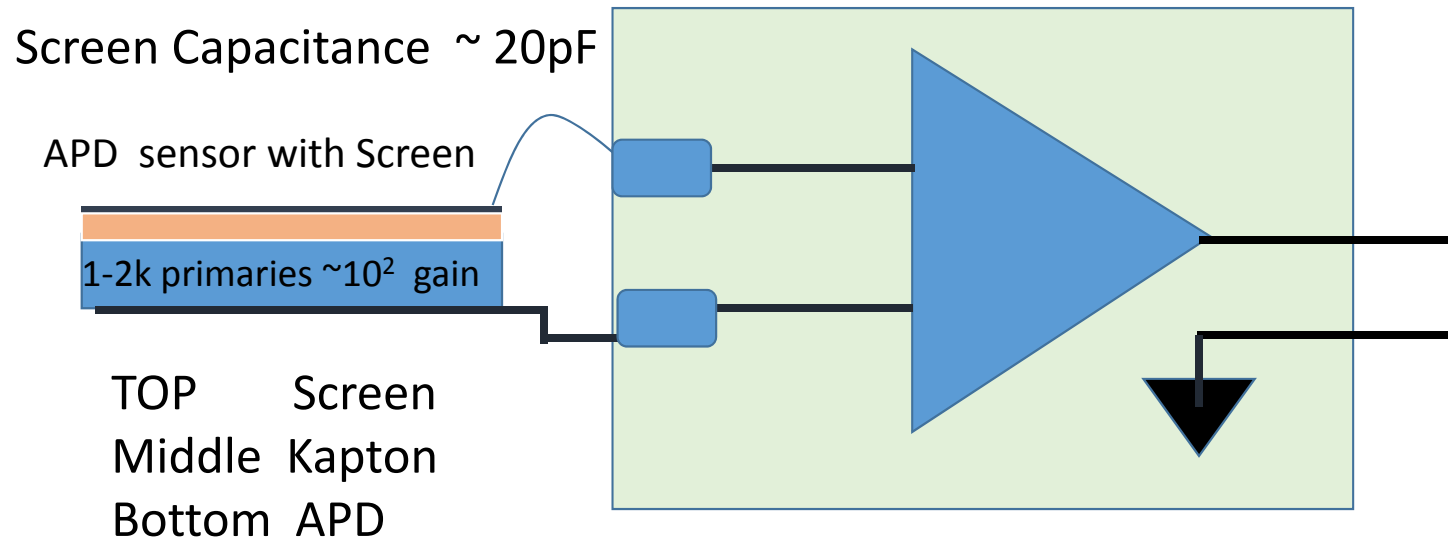
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February 2017

APD with Screen Readout



Two basic Approaches to detector readout

High Z amplify the voltage on the Detector

Low Z Transfer the charge to the Preamplifier

Approach for readout

High Z - Signal stays on detector

Voltage Readout $\Delta V \rightarrow Q/C = 1e-15/20e-12 \rightarrow 50\mu V/fCoul.$

To amplify this up to one $\sim 1mV$ V_{out}/V_{in} one stage $\sim 20X$ ($1mV/fC$ suitable to pass to next amp stage)

To meet a target $\sim .5ns$ rise $\rightarrow 14GHz$

Hard to imagine steering enough current through the input stage without at least charge sharing eg. Matching the detector capacitance with input transistor capacitance which inherently limits bandwidth.

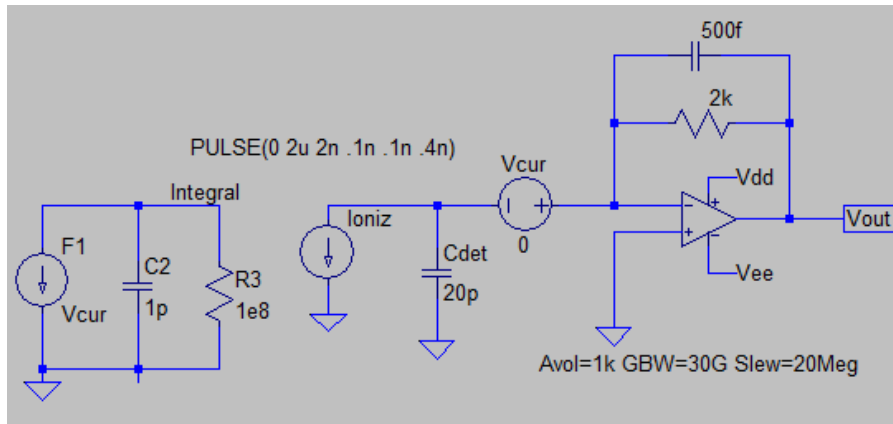
Low Z - Signal Charge Drained from detector through feedback and placed on amplifying node.

- Good Signal to Noise requires both low noise circuit design and a technique to transfer the signal into the amplifier within the expected peaking time.
- Design issue is to understand how to maximize signal transfer.

Cdet pF	Rin Ω	% signal
20	50	47%
10	50	71%
20	10	94%
10	10	99%

% Signal collected in Amplifier
with 200 ps wide signal + .5ns peak

Ideal Low Z Readout 30GHz GBW



APD Signal Goal $\sim 50 - 150\text{fC}$ (gain dependent)

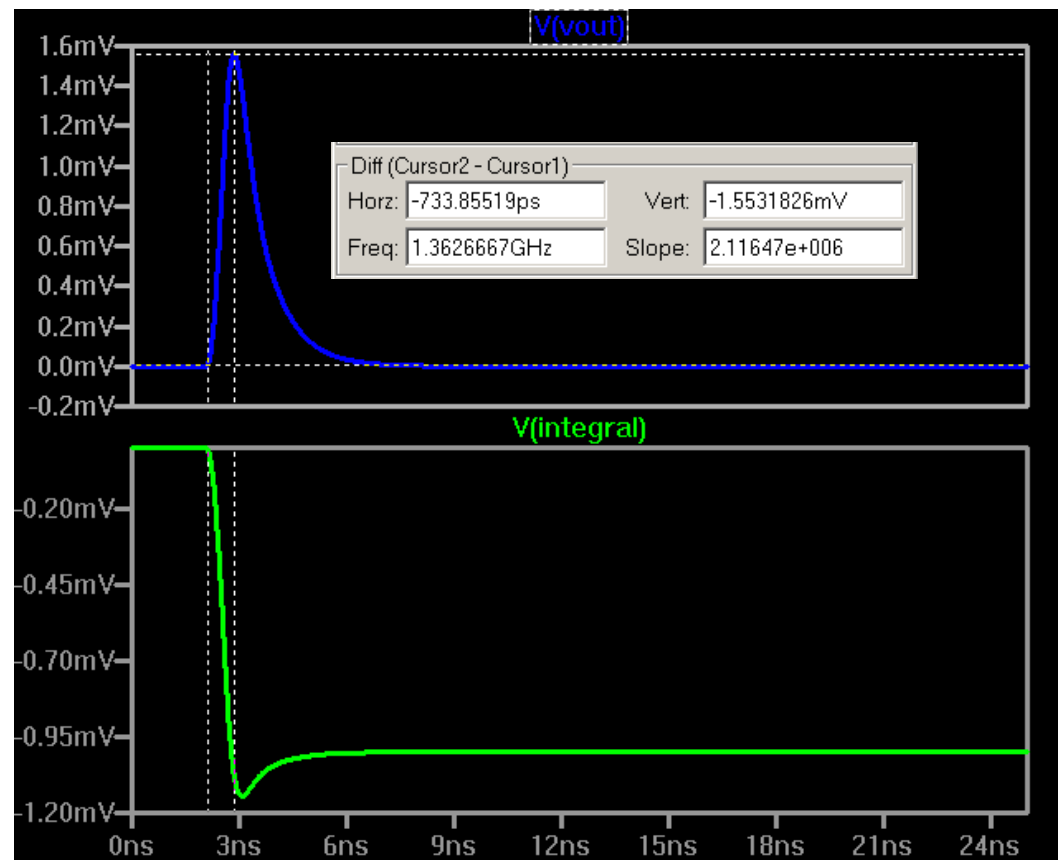
Acquire > 90% of the signal in peaking

Signal to noise $\sim 100:1$

Peaking time $\sim 1\text{ns}$ or faster

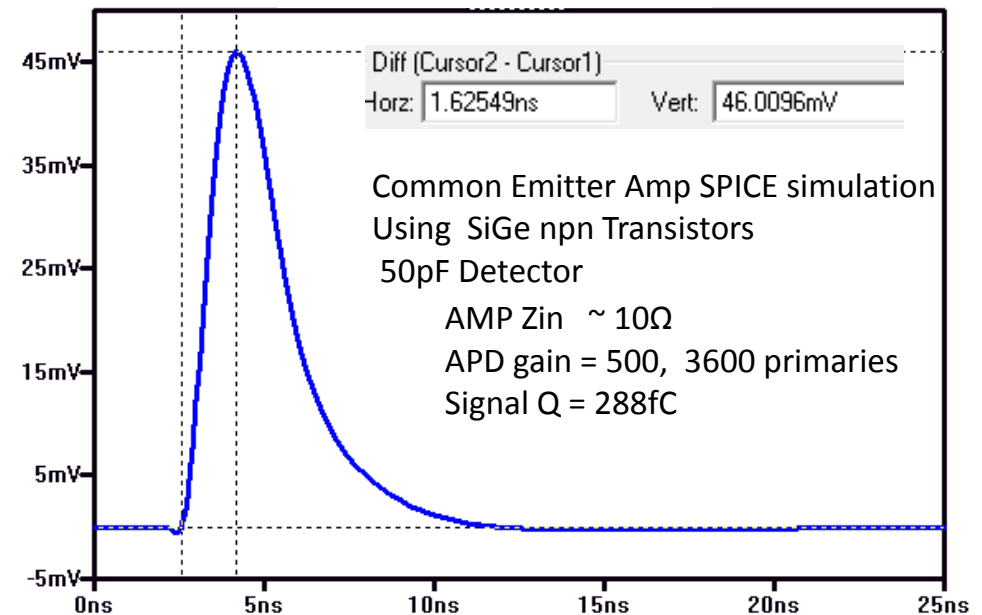
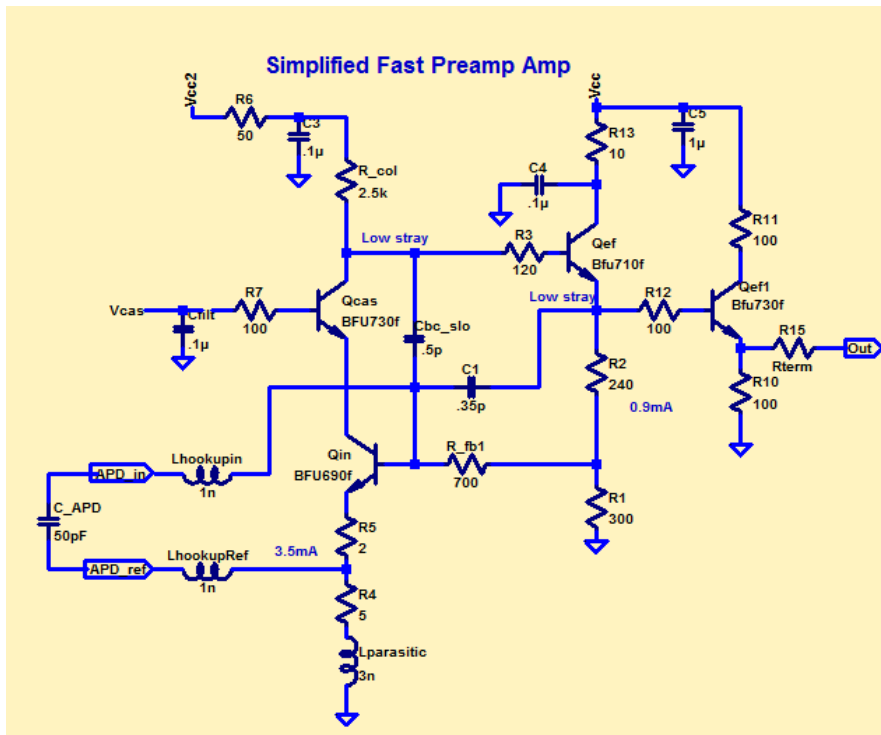
Primary objective is to provide a prototyping

Amplifier to characterize the APD (or LGAD) signal.



First Ideas..... Common Base → Common Emitter... →

Preamp Out AC_Vout

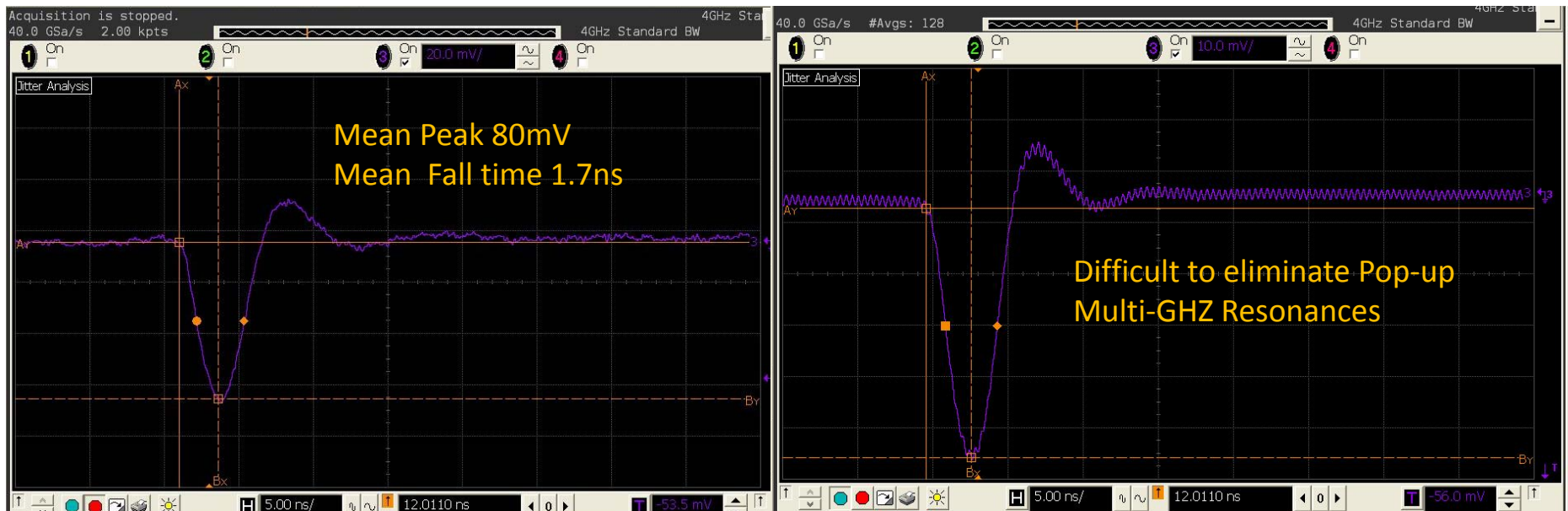


APD Preamp Objectives ~1ns Risetime, Low (series) noise

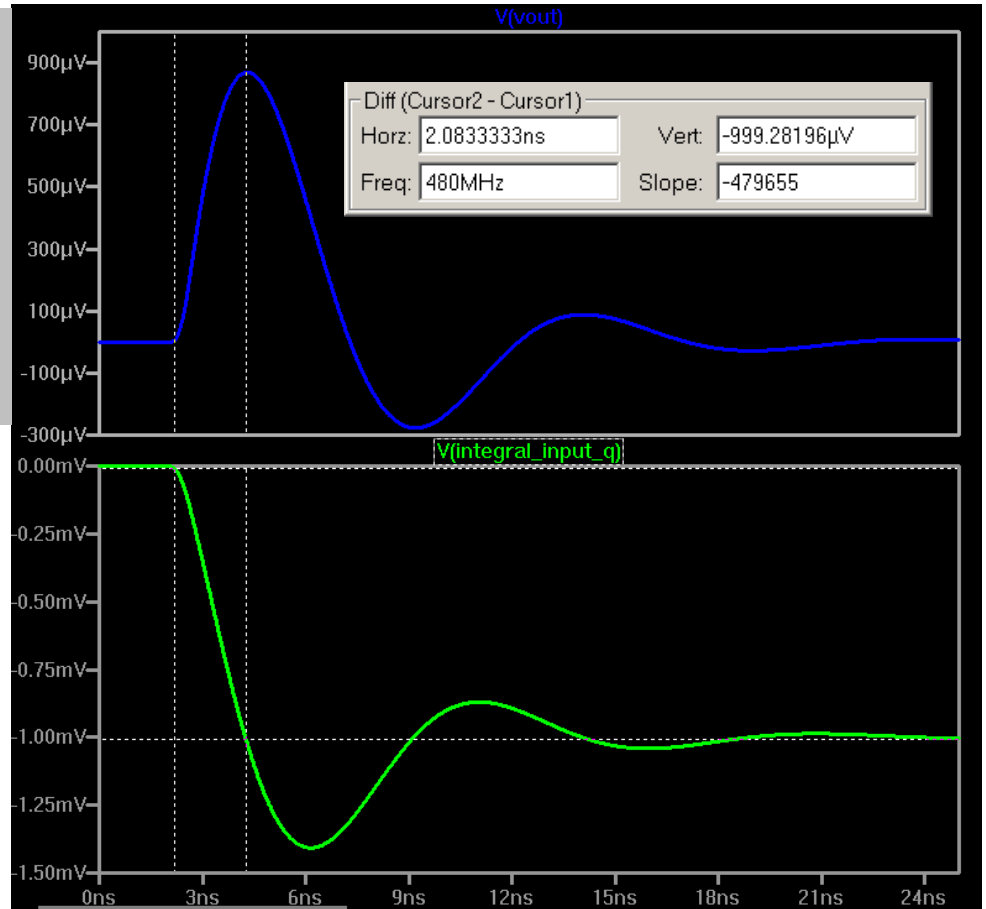
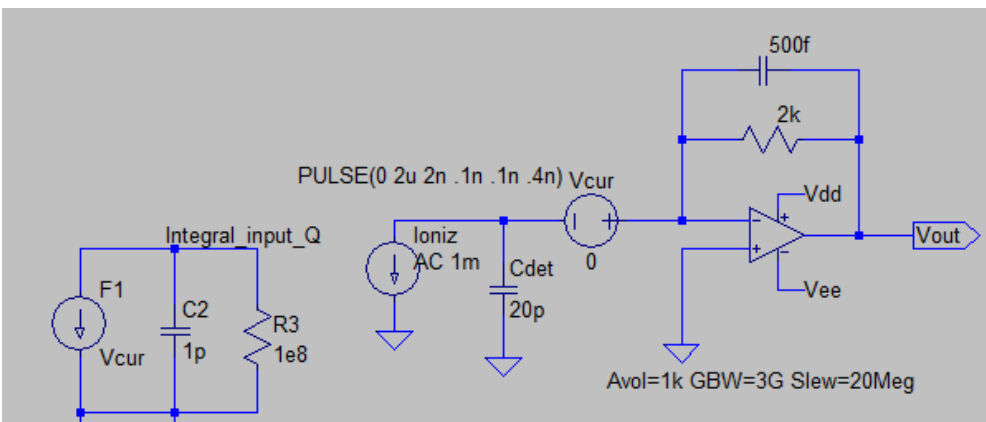
- Low $R_{in}C_{Total}$ Time Const. → Remove as much charge as possible APD
Fast APD signal $R_{in}C_{Total} \approx 1ns \rightarrow R_{in} \sim < 20\Omega$
- Limit Amplifier Series Noise Use Low $r_{bb'}$ bipolar Input transistor.
- Gain BW ~ >1GHz → Choose Fast Bipolar Transistors
- Connections Short, Low inductance → Amplifier within CM of detector

Fast Timing APD Amplifier RD51 Report February 2017

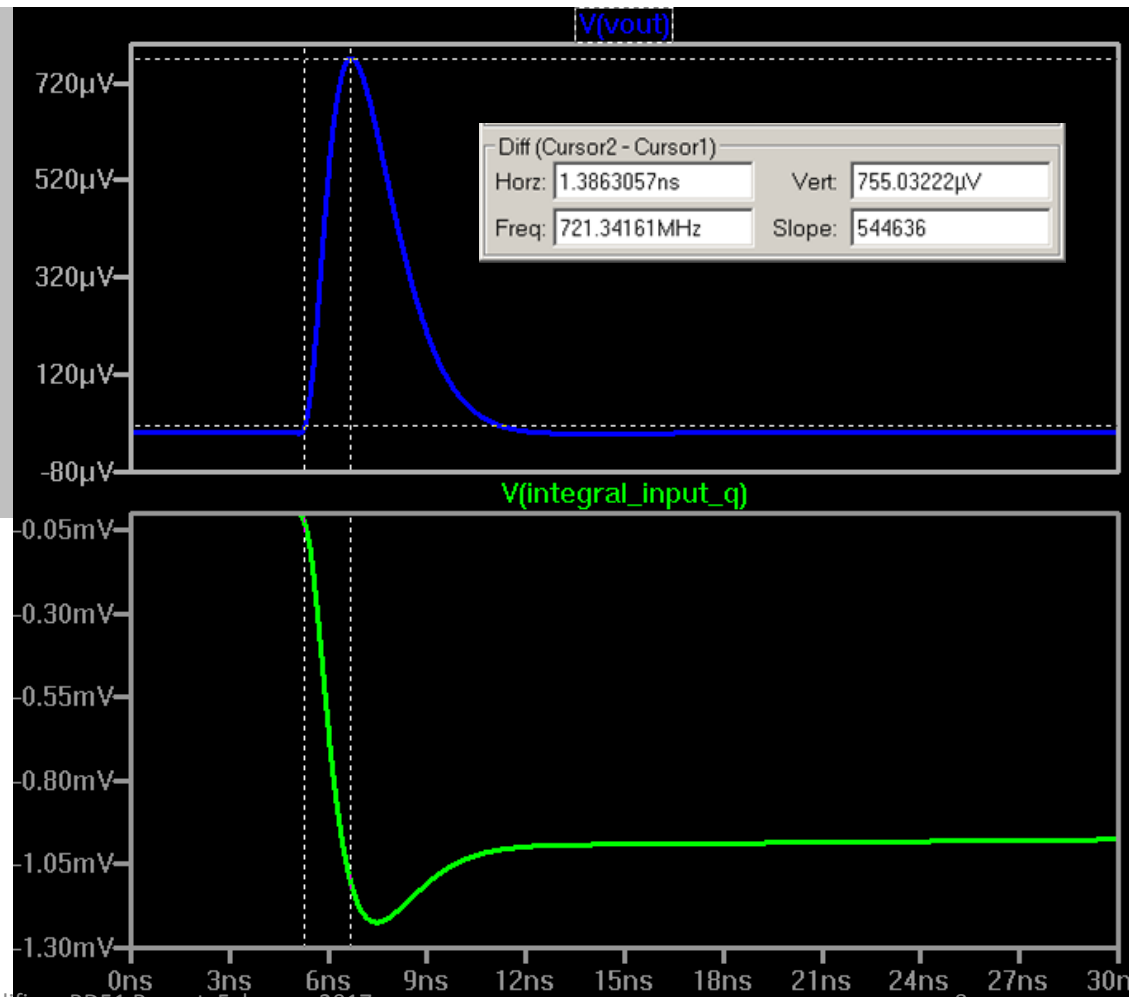
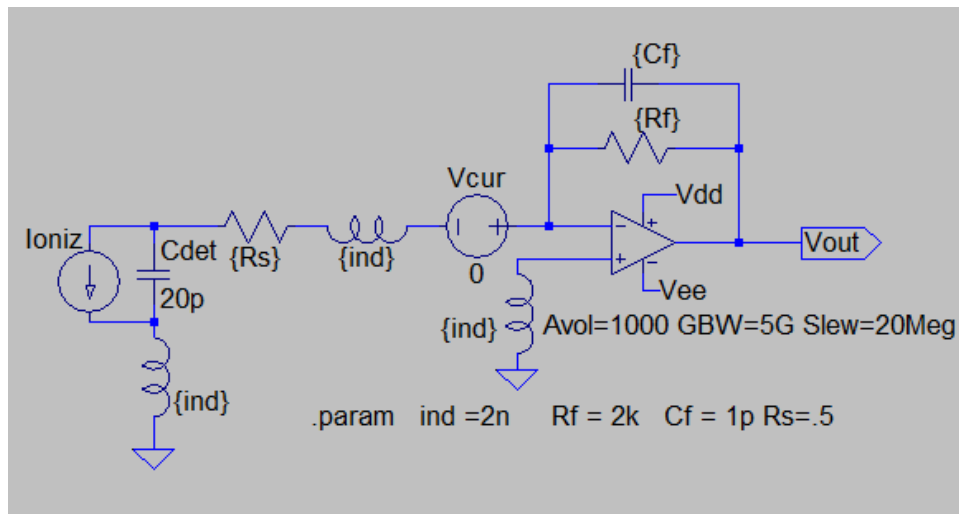
Discrete Amp response to Fe55 Source



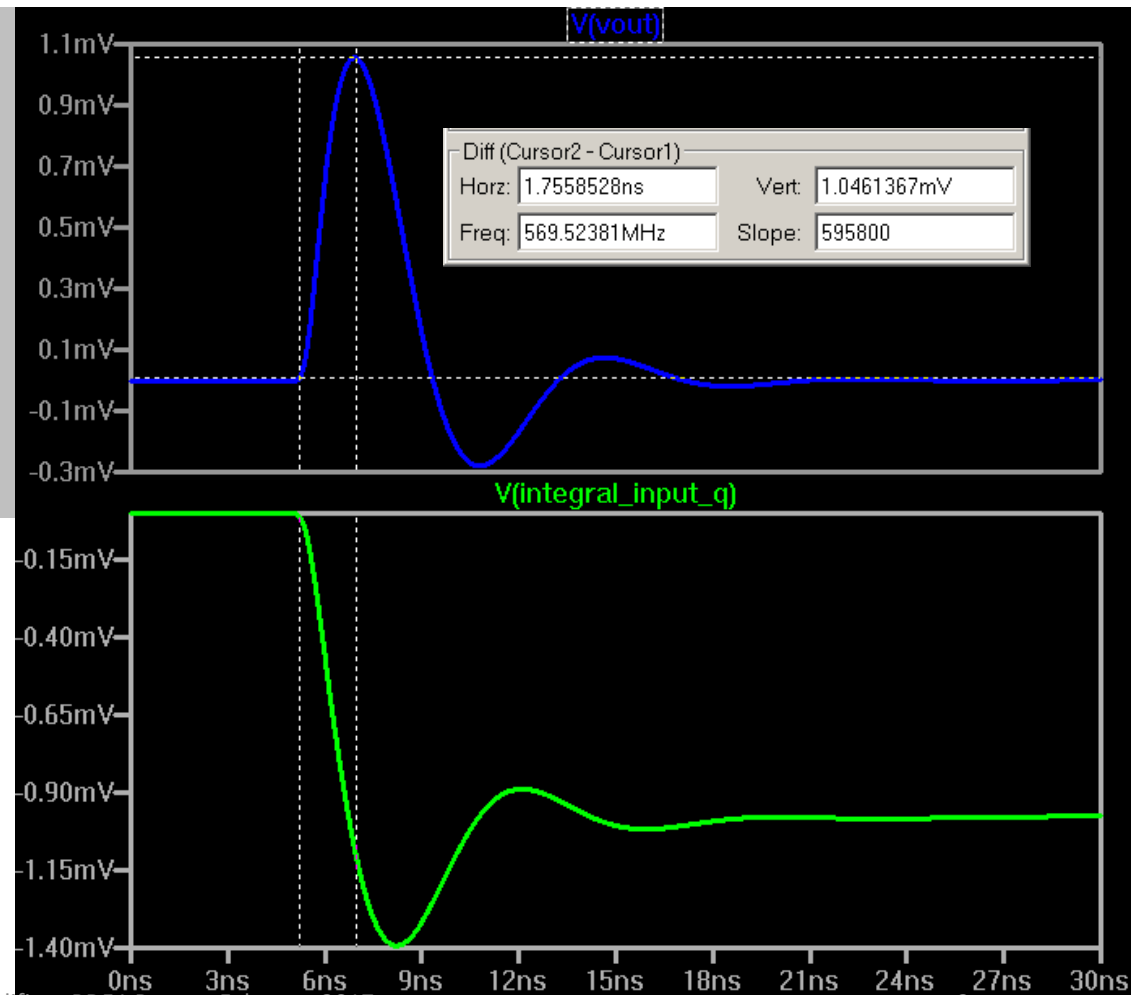
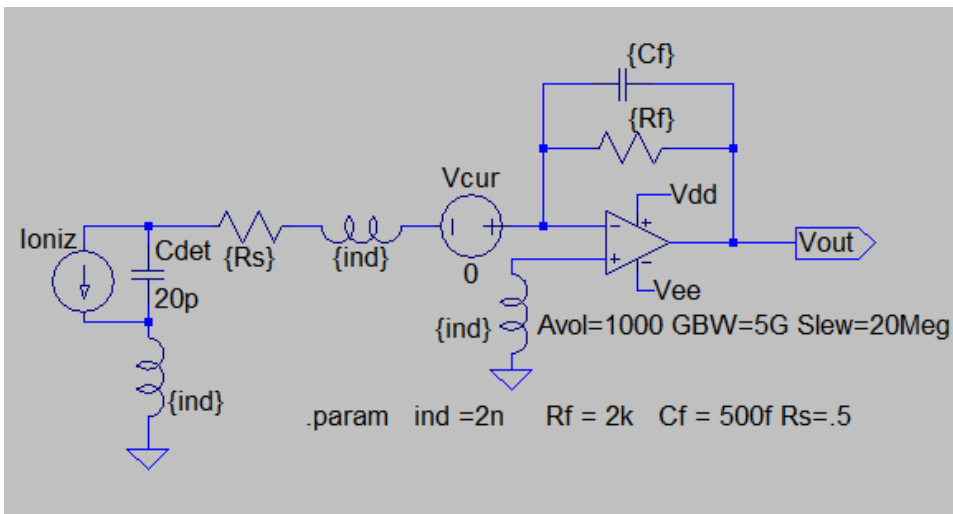
Low Z Readout 3 GHz GBW



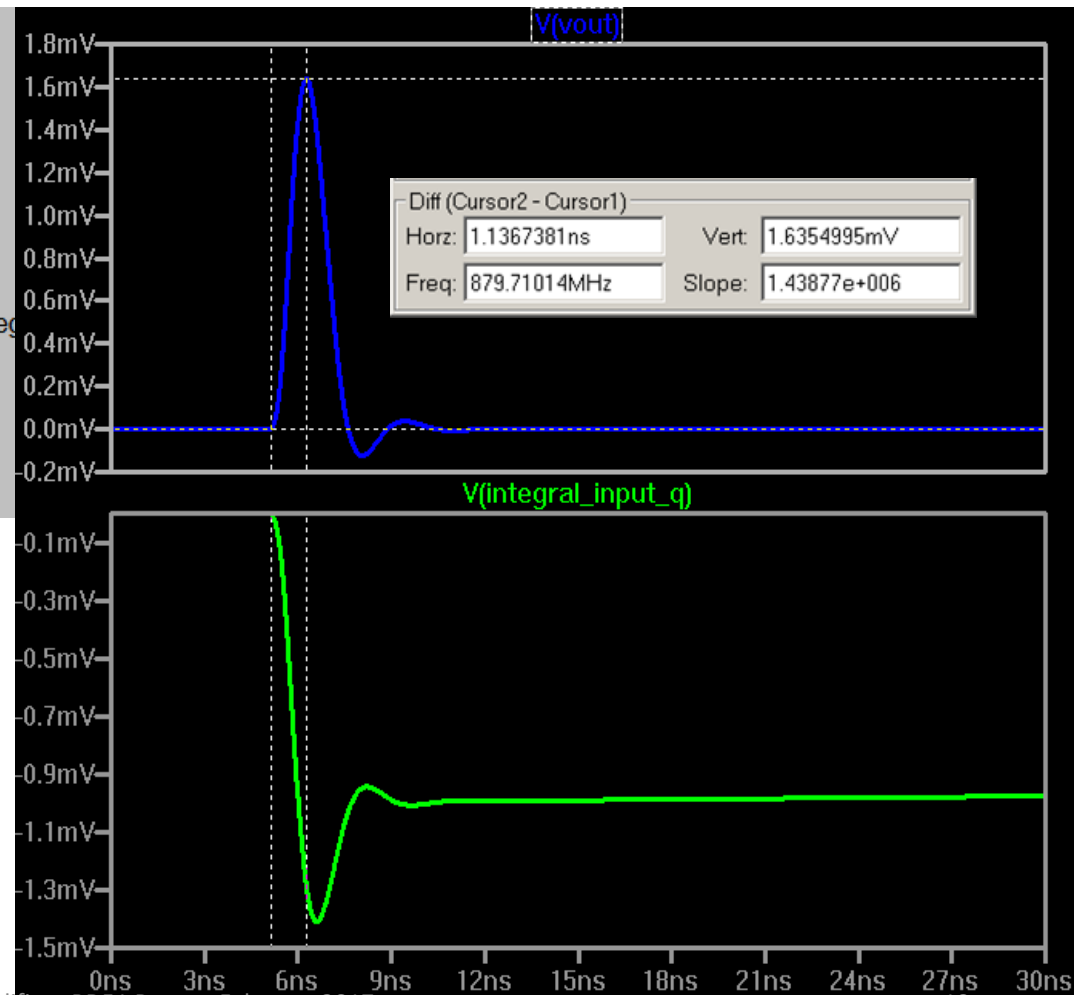
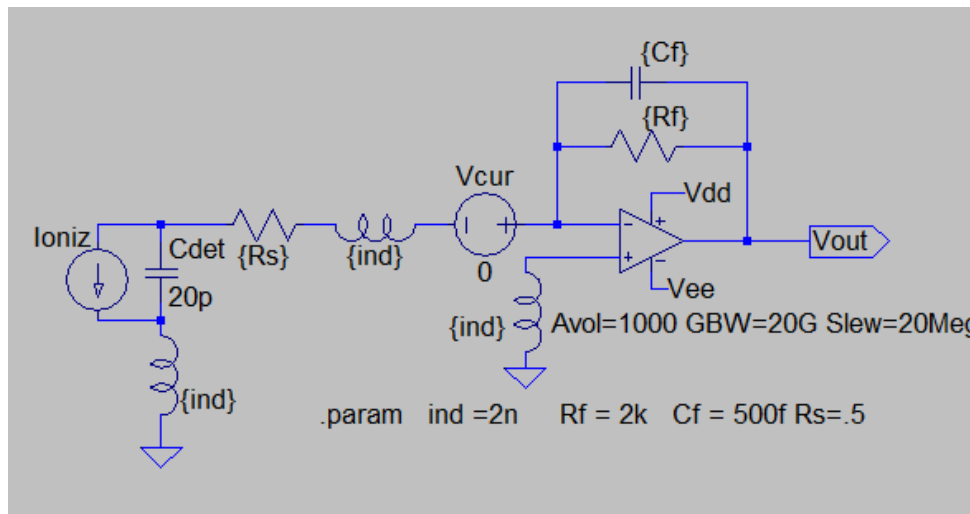
Low Z Readout with hookup Parasitics 5 GHz GBW



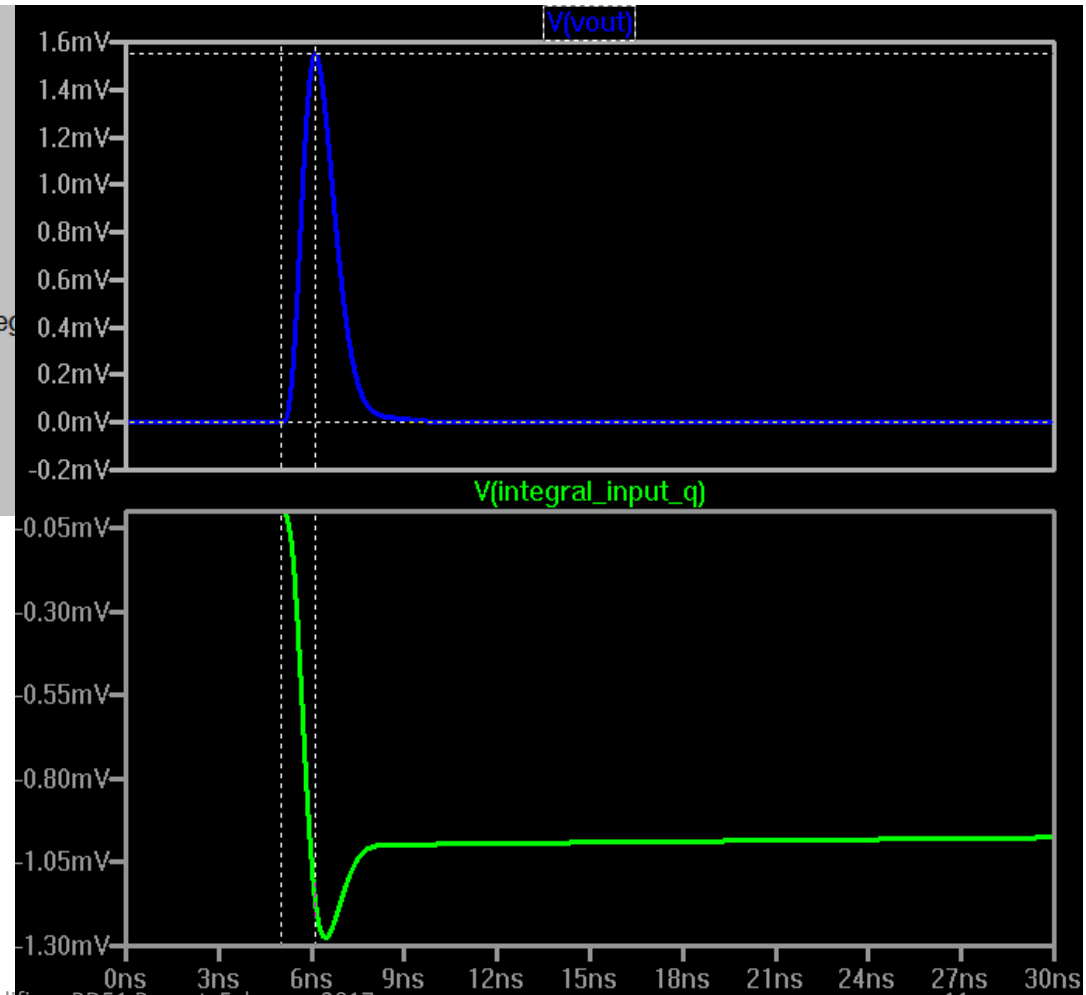
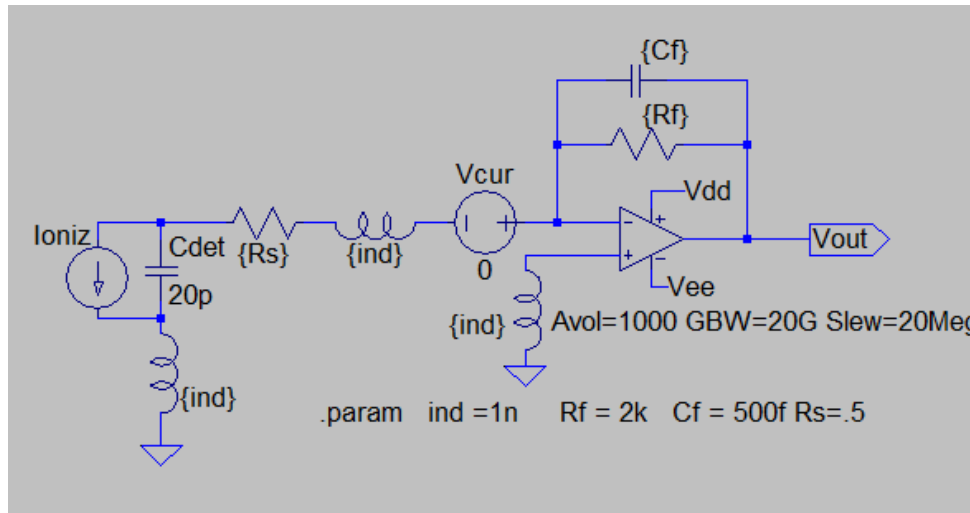
Low Z Readout with hookup Parasitics 5 GHz GBW



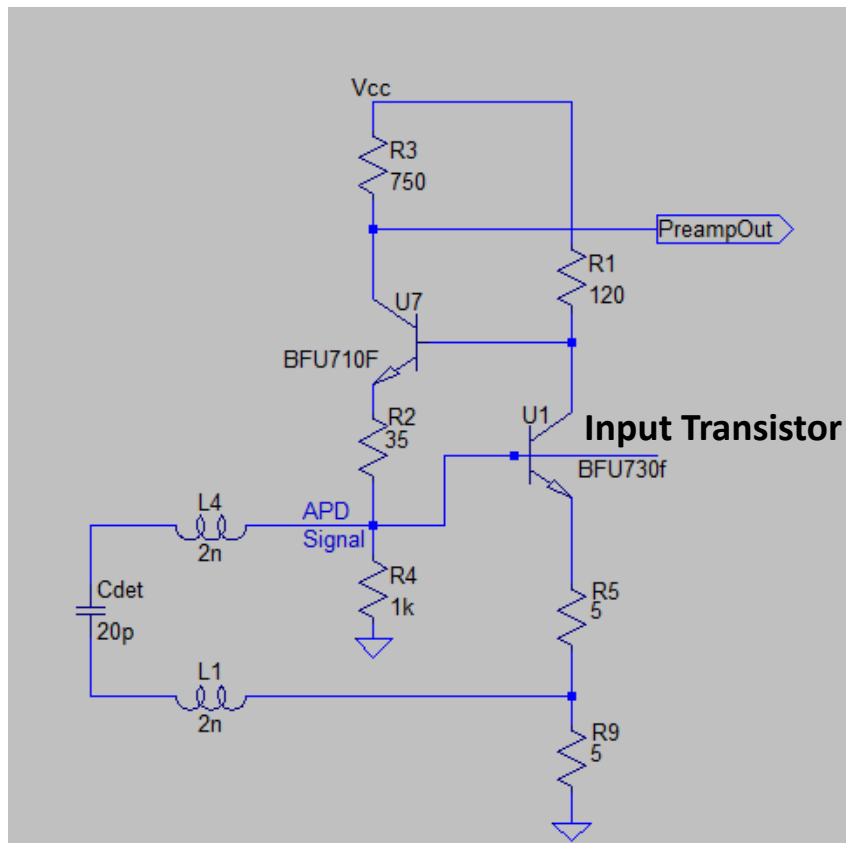
Low Z Readout with hookup Parasitics 20 GHz GBW



Low Z Readout with hookup Parasitics 20 GHz GBW

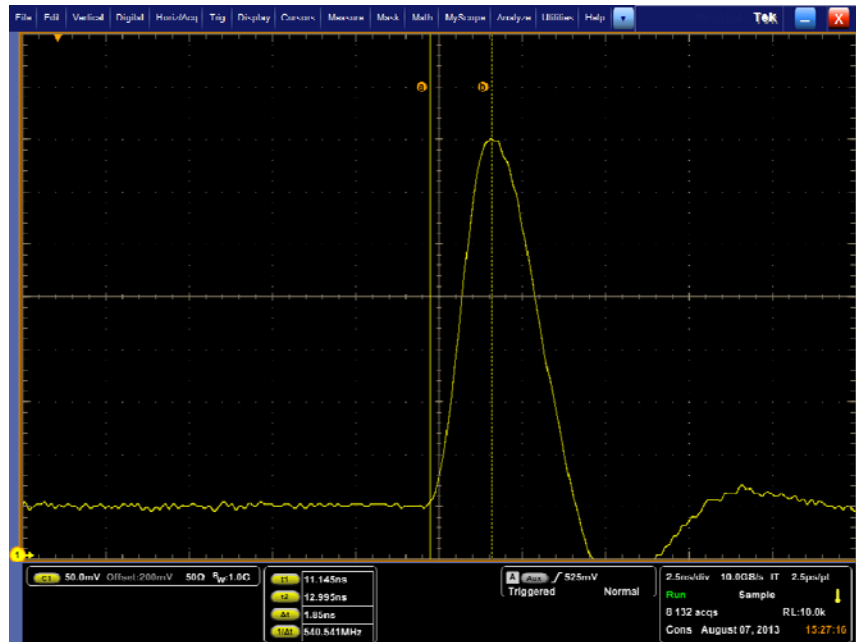
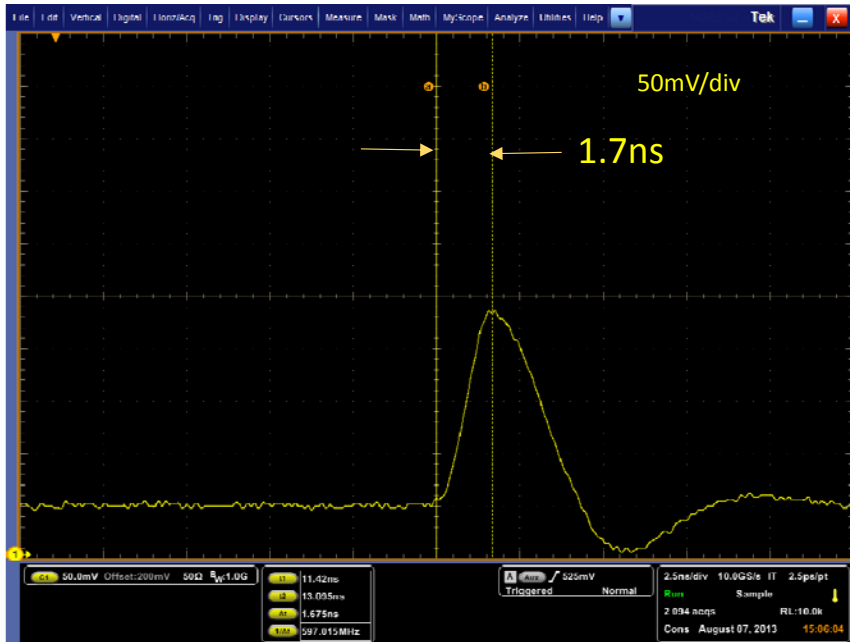


Super Beta Preamp Configuration

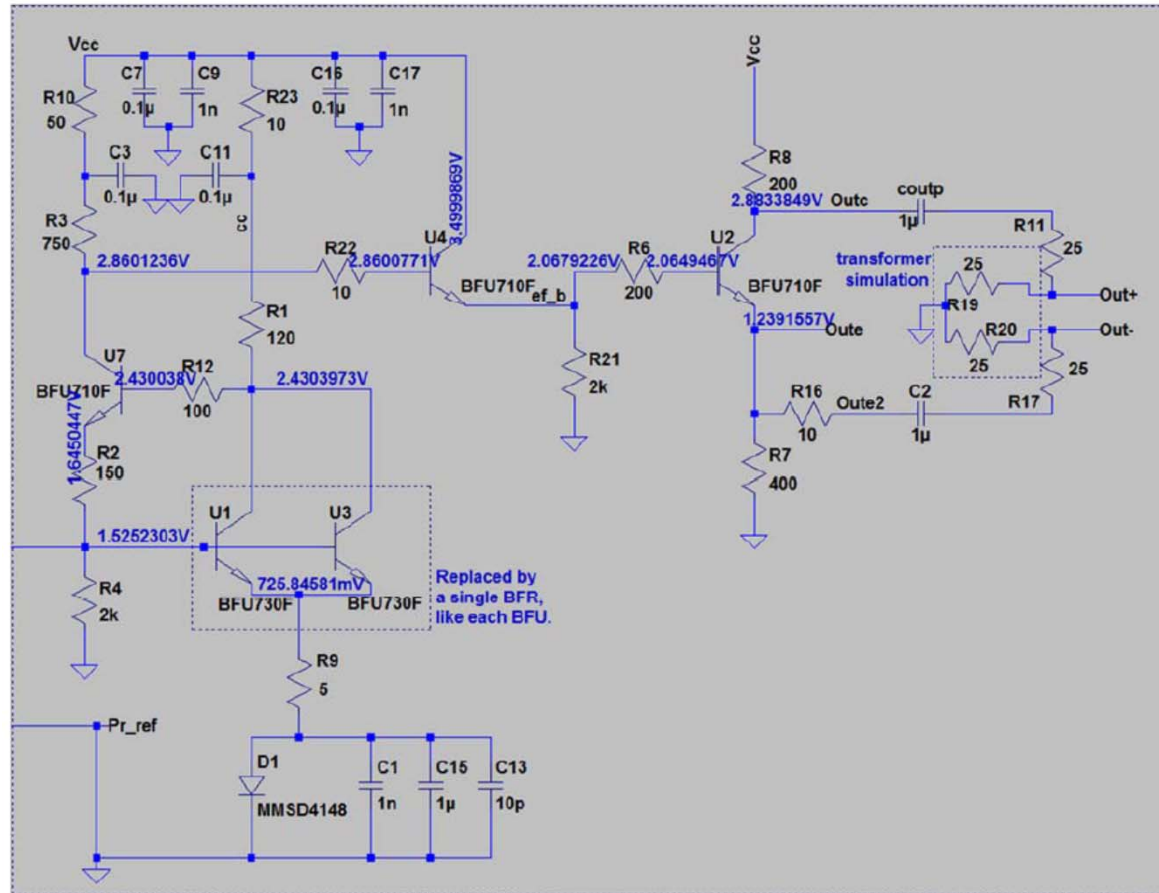


Very Low input impedance
Fast Response with SiGe Transistors
Preamp output ~ few mV/fc

Sample Measurements fast pulser input to AMP.

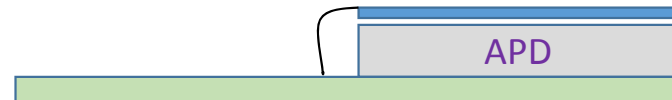


Discrete Amplifier Design with Differential Output

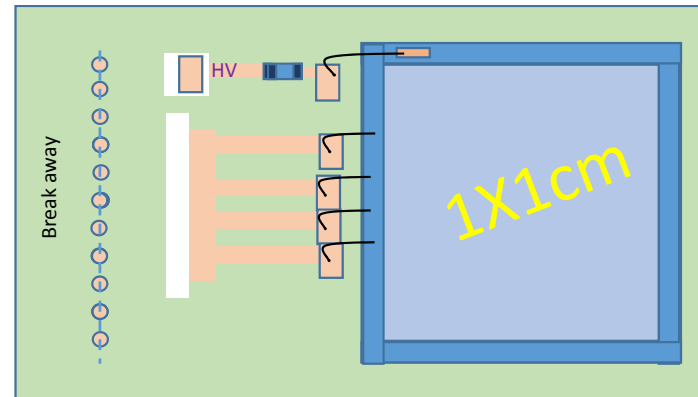
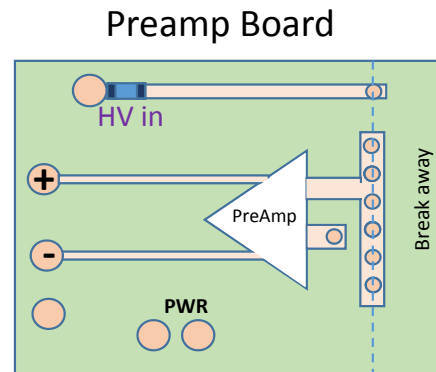


Physical Implementation APD on Translation Board

Notional Implementation

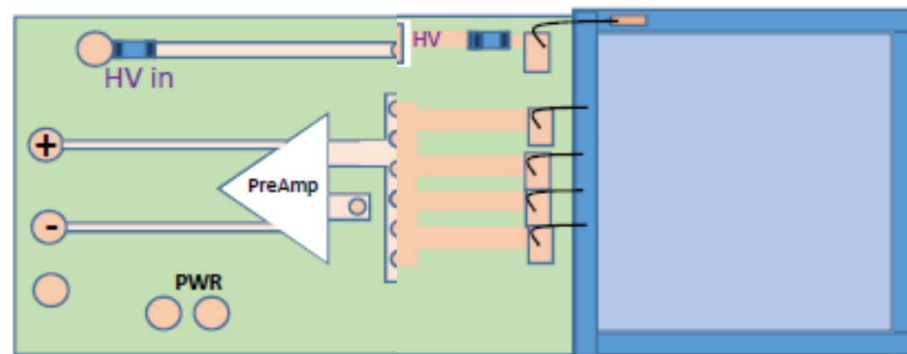


APD Fixture

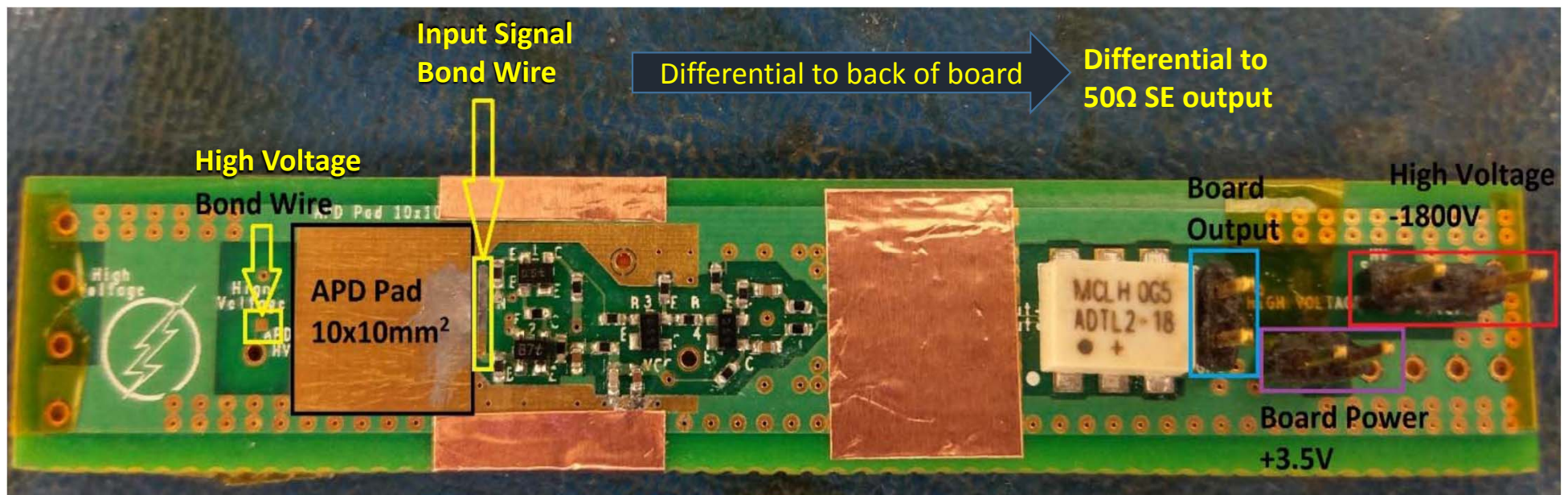


APD on Translation Board With Preamp Solder Attached

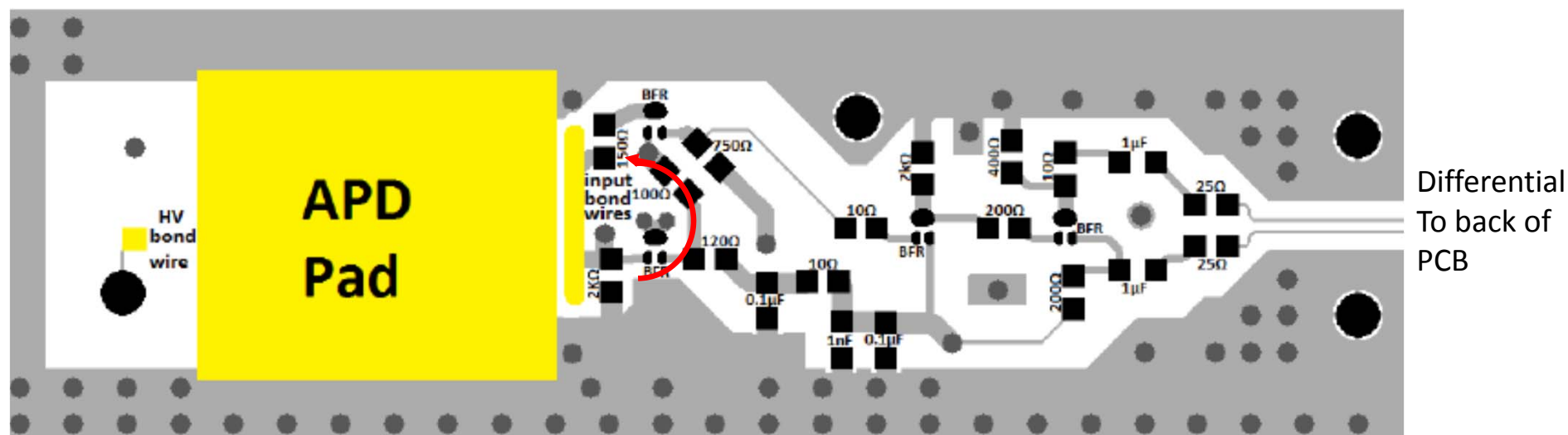
Notional Implementation



Realized PCB Stuffed Amplifier Board.

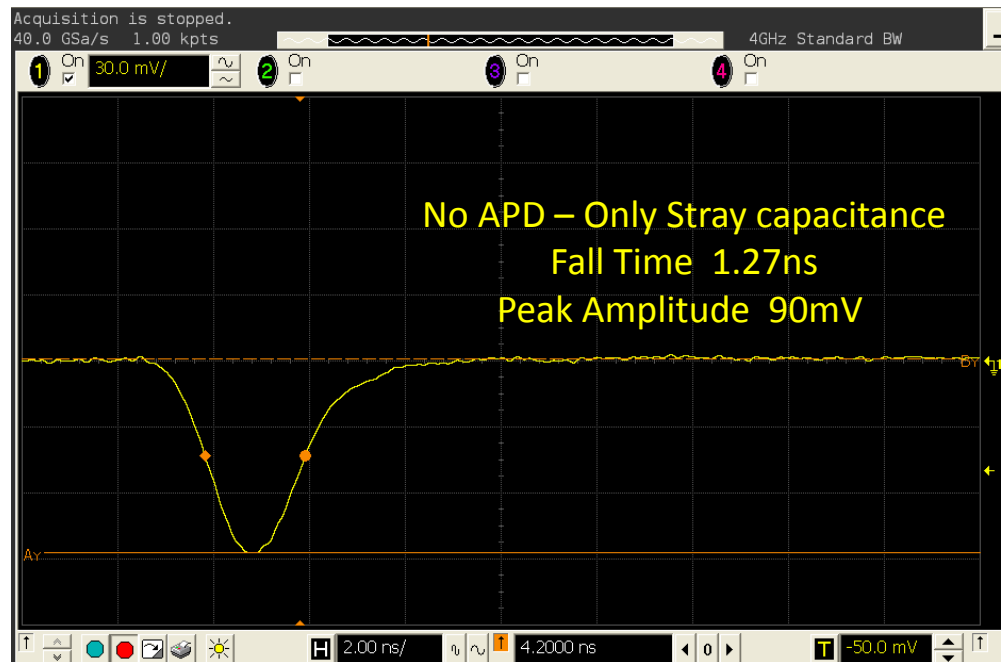


The feedback path still contributes significant delay into the charge restoration on the detector.



Measurements of Preamplifier using Pulser input 1ns Rise/fall 120fC pulse 50 ohm load into Scope

Input Transistor Current 11.6mA



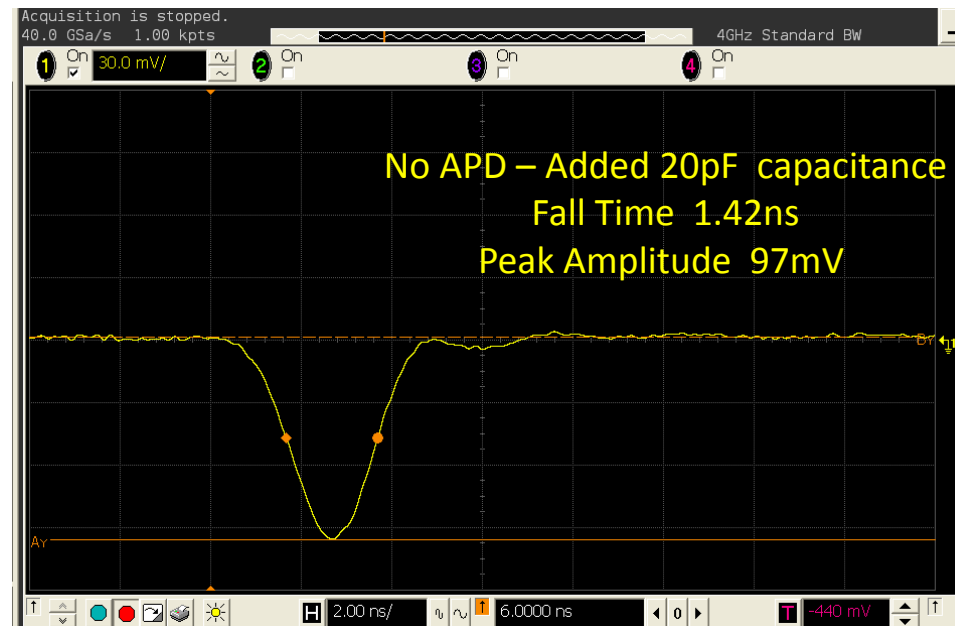
Measurements with Pulser 1ns Rise/fall 120fC pulse 50 ohm load into Scope

Input Transistor Current 11.6mA



Measurements with Pulser 1ns Rise/fall 120fC pulse 50 ohm load into Scope

Current of input transistor increased by 2.5mA



***STATUS Feb 2017:* Waiting for Opportunity to readout with biased APD**

ASIC Version of Fast Amplifier for Prototyping

- Design intended ONLY to improve understanding of APD signal.

Goal: Port signal from sensor to prototyping friendly environment

Amplify & buffer sensor signal without compromising bandwidth transforming it from a low impedance input to a differential 50Ω cable compatible output.

- Input Impedance $\sim 10\Omega$
 - Noise $\sim .5\text{fC}$ for a 20pF input
 - Sub-ns output rise time 500-600pS impulse response
 - 5mV/fC differential gain
 - 4 channel device suitable for Tile Construction
- NOT intended for High Radiation environment

Rather to point out requirements for a successful Rad Hard process.

Additional Features

Pseudo Differential Input has a potential 40% intrinsic noise hit

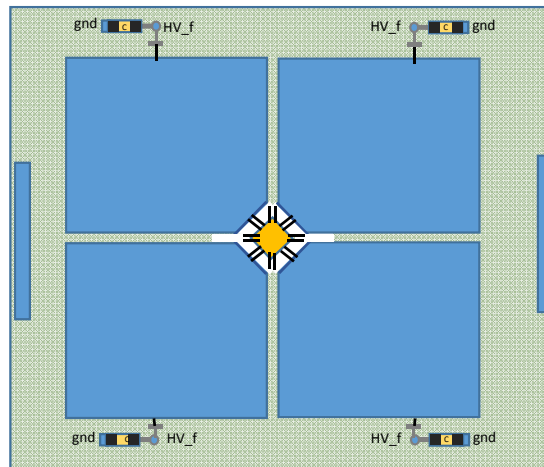
- Offers common mode input protection,
- Potential for differential sensor hookup
- Dual Gain $2\text{mV} \rightarrow 5\text{mV} / \text{fC}$
- Moderate power requirement $\sim 50\text{mW}$ per channel.

Very Notional sketch Front and Back of APD (or LGAD) Array

Board view from backside is transparent for visualization

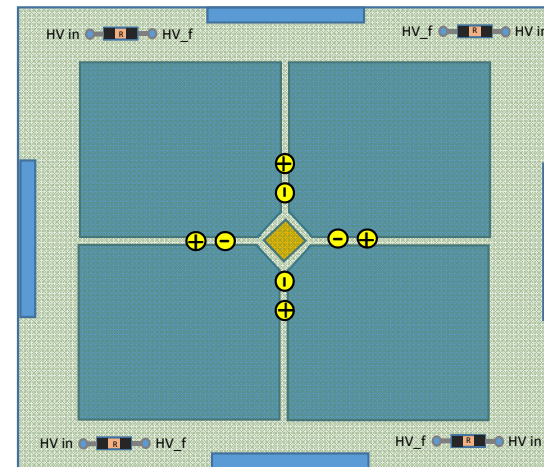
Front View

4 Channel Readout ASIC on front
No External connections this side



Back View (back of PCB)

Readout/HV/PWR
Amplifier Signal Routed out on back



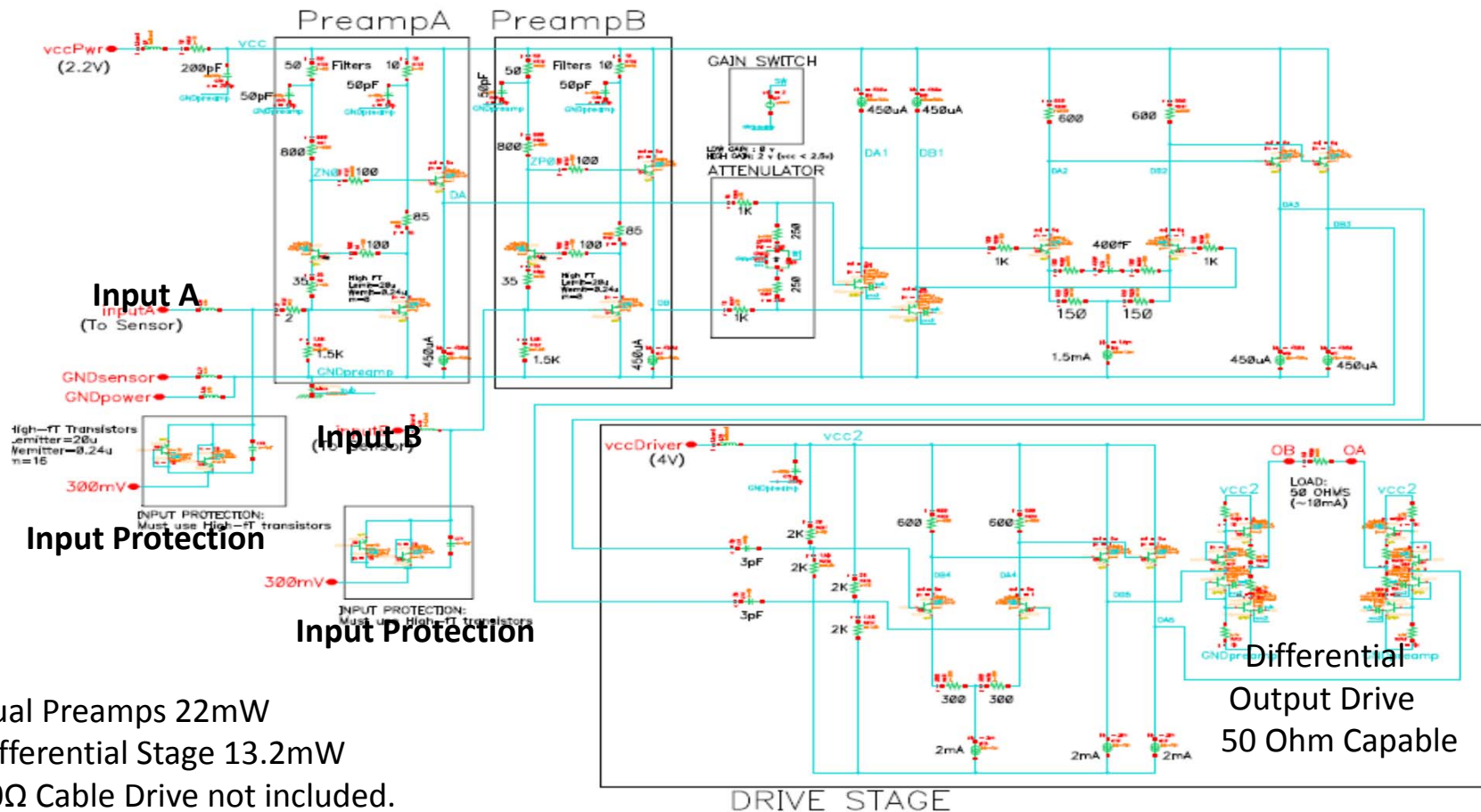
Reference Pads

4 Channel PREAMP ASIC is on same PCB gnd plane as Sensors
NO connections from noisy environment on Front side

An Interesting proposal
from Bert Harrop at
Princeton suggests
A BGA packaging
For the APD's

7WL Silicon Germanium Bi-CMOS Preamp

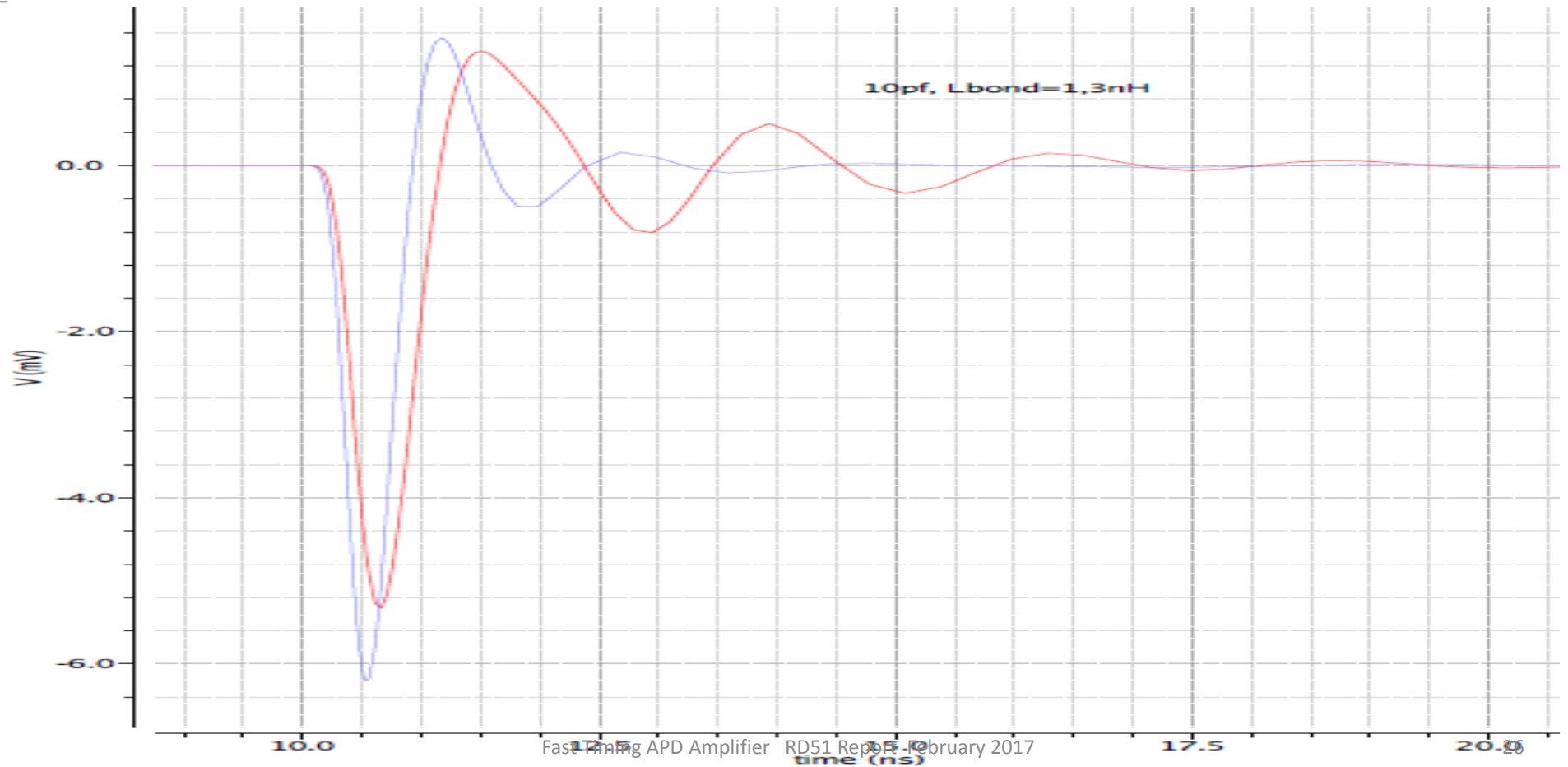
GAIN: 5mV/fC , INPUT IMPEDANCE ~ 10 Ohms NOISE: ~0.5fC



Dual Preamps 22mW
Differential Stage 13.2mW
50Ω Cable Drive not included.

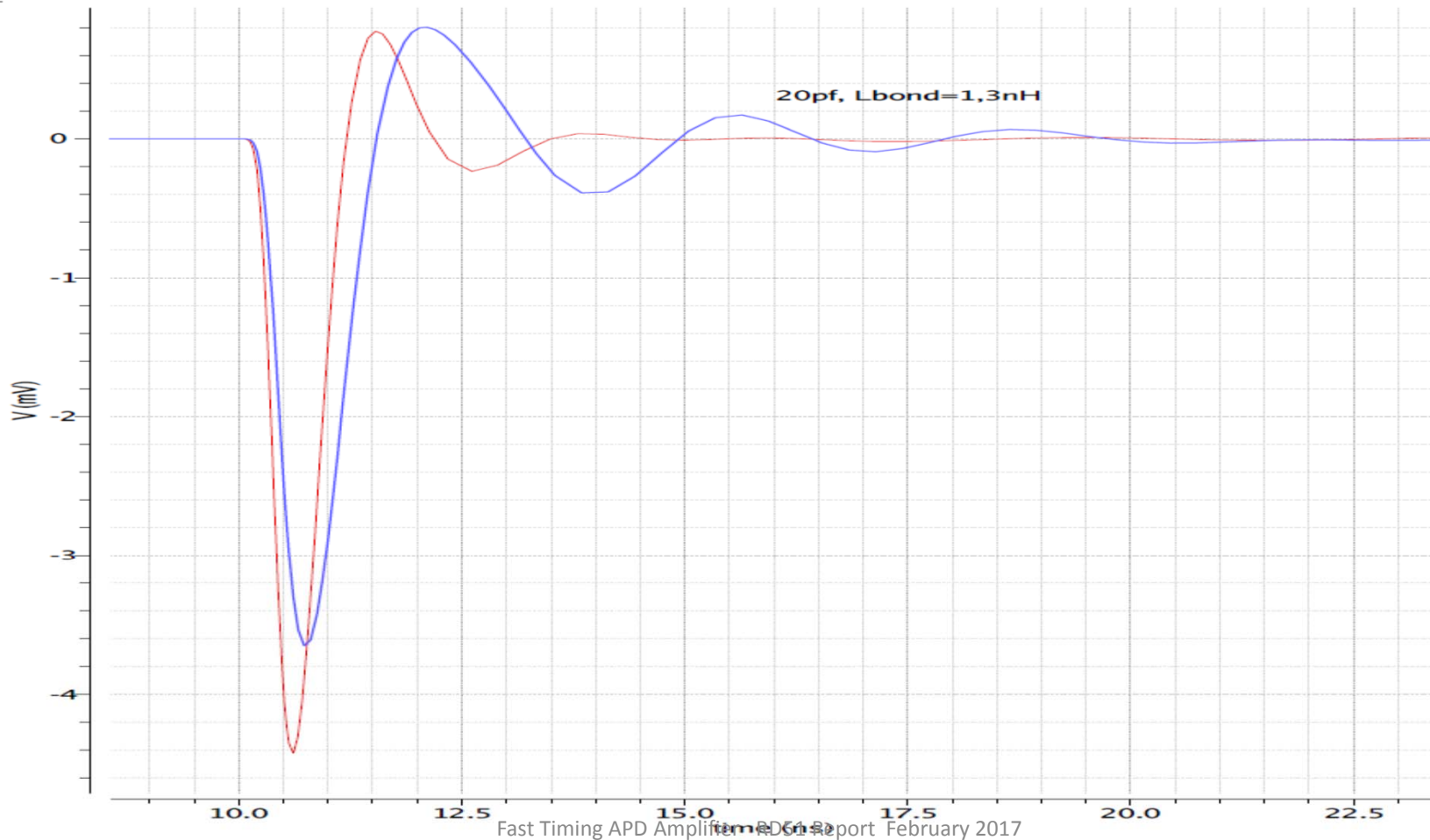
Impulse Response for 10pF capacitance

for 1nH (blue) and 3nH (Red) Detector hookup



Impulse Response for 20pF capacitance

for 1nH (red) and 3nH (blue) Detector hookup



ASIC Status

- Schematic Design largely complete
- Target: March Submission, Layout in progress
- Awaiting NDA signatures for updated design 7WL kits

Summary

We have been exploring Fast preamplifier Readout of moderate capacitance (10 - 20pF) APD sensors.

- Signal quality depends on:
 - Low input impedance to get the Signal into the amplifier.
 - Amplifier Gain Bandwidth
 - Low Noise
 - Packaging (inductance/proximity/pickup)
- ASIC prototyping amplifier in SiGe should have plenty of bandwidth and allow tests with tiled detectors in several configurations.