June 12, 2015

PENN Fast Amp for CMS Detector at CERN

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Board 1

The top layer of the board looks like this:

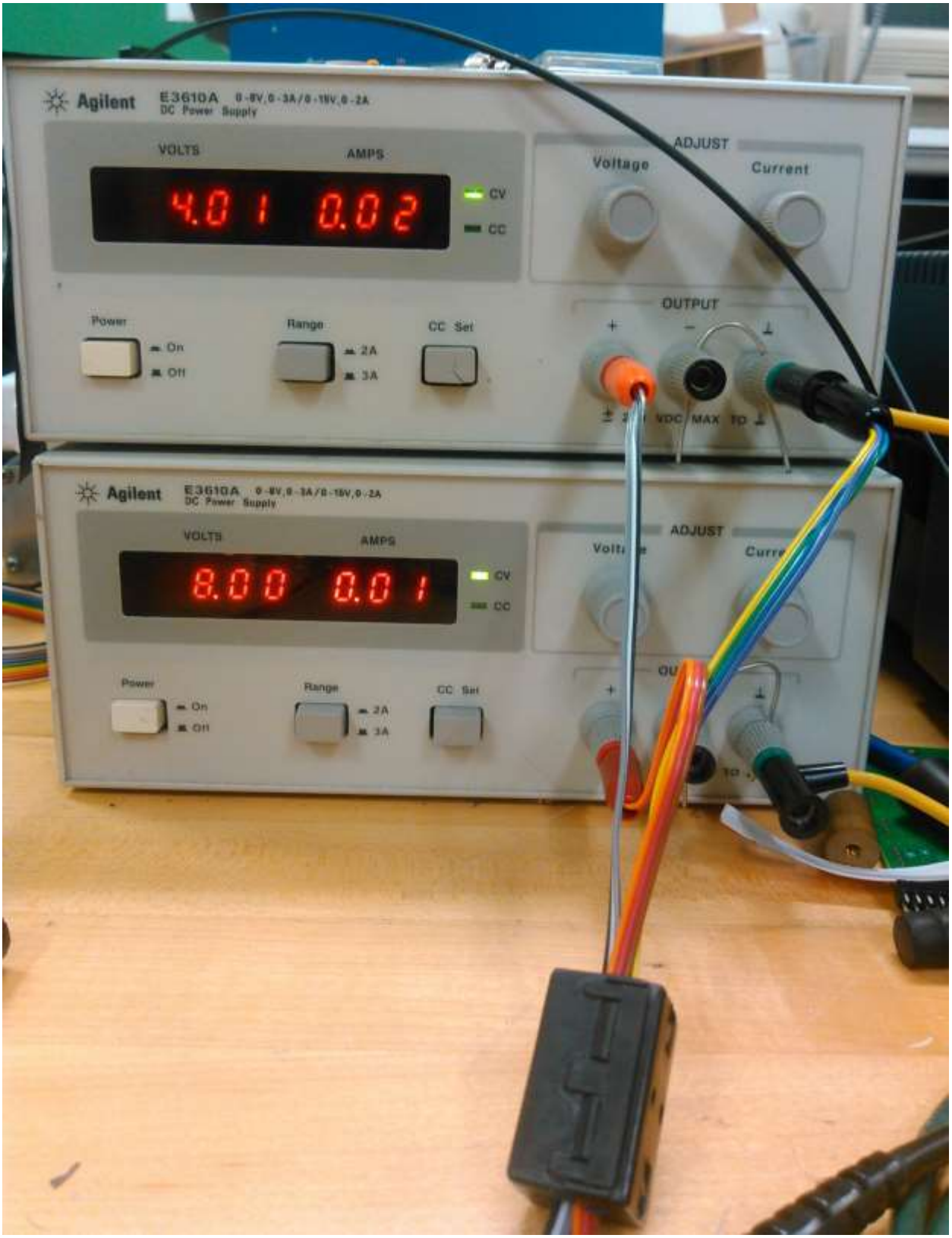
Visible modifications on the board are:

- A 0.2 pF capacitor was added between the collector for U2 and ground using a wire because there is no pad for the C13 on the LTSpice schematic.
- A 1pF capacitor is soldered into the APD input signal that is used for the pulse generator's input signal.
- Piece of copper was soldered on the ground pad on the top layer of the board, covering the bottom around the input side of the circuit. More pieces of copper were added to form a rectangular wall that isolates the first three transistors from the rest of the circuit. Also, the ground from the input has a strip of copper soldered into that makes contact with the brass box, in order to help keep the signal from oscillating.
- On the output side of the board, multiple copper strips were used to cover the circuit because there was still some oscillation at the output, while the board was only being powered.
- Both output and power cables were wrapped in copper to prevent the noise generated by the power cables from creating oscillations at the output. Also, ferrite cores were attached to the power cables inside and outside the box to put an end to the oscillations observed at the output. The ferrite core inside the box made the biggest difference and cleaned out the output signal.

More pictures of the board and the setup:

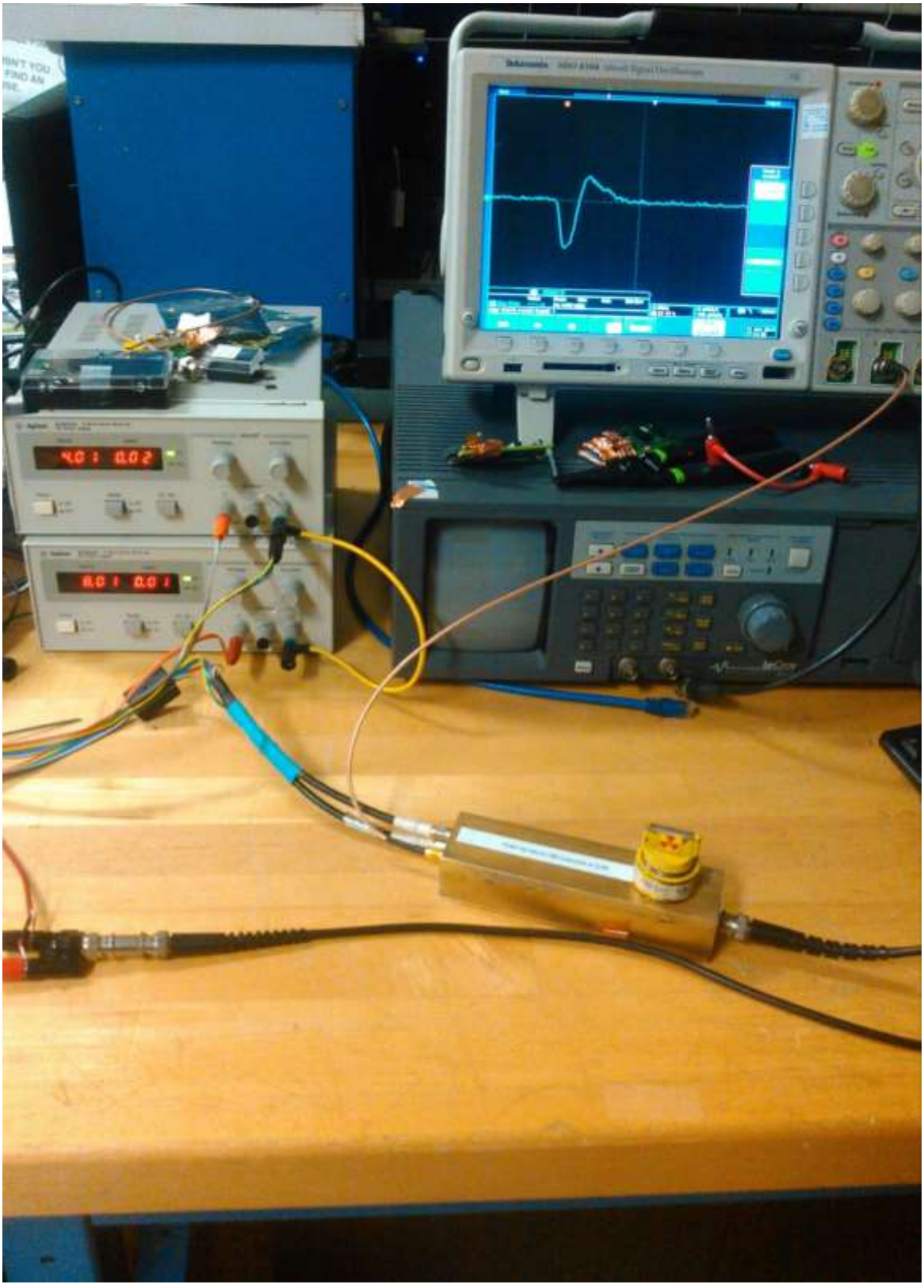
Close-up of the output side.

Close-up of the input side

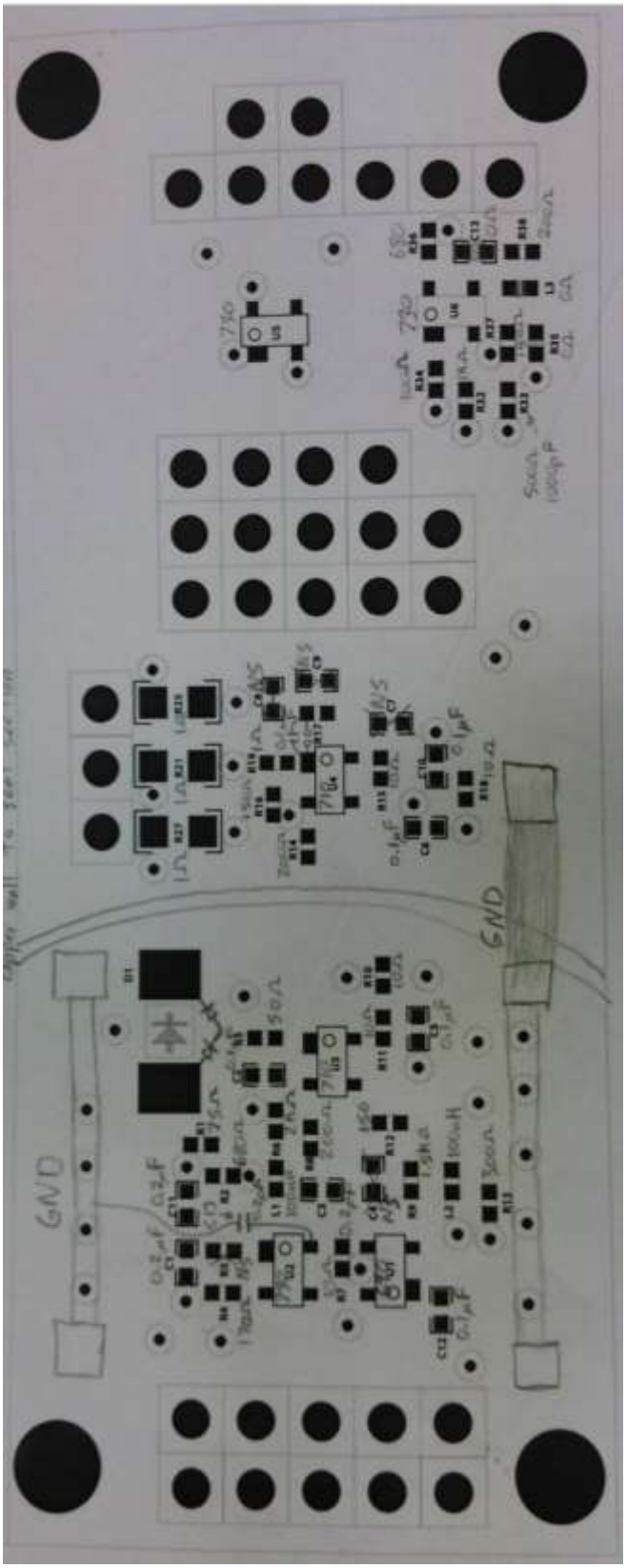


Supply voltages used to power the board

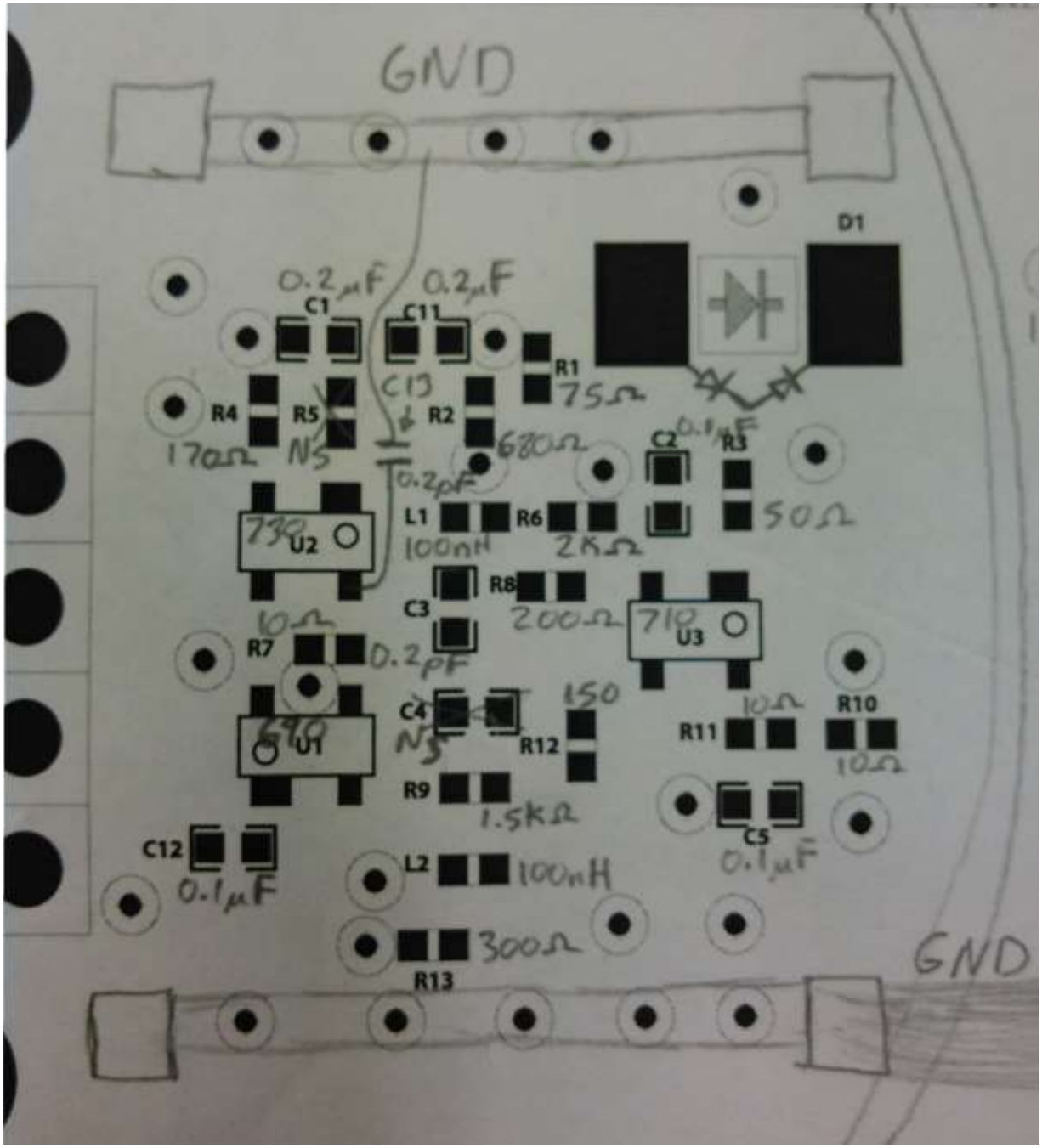
High voltage supply set to -1.75kV



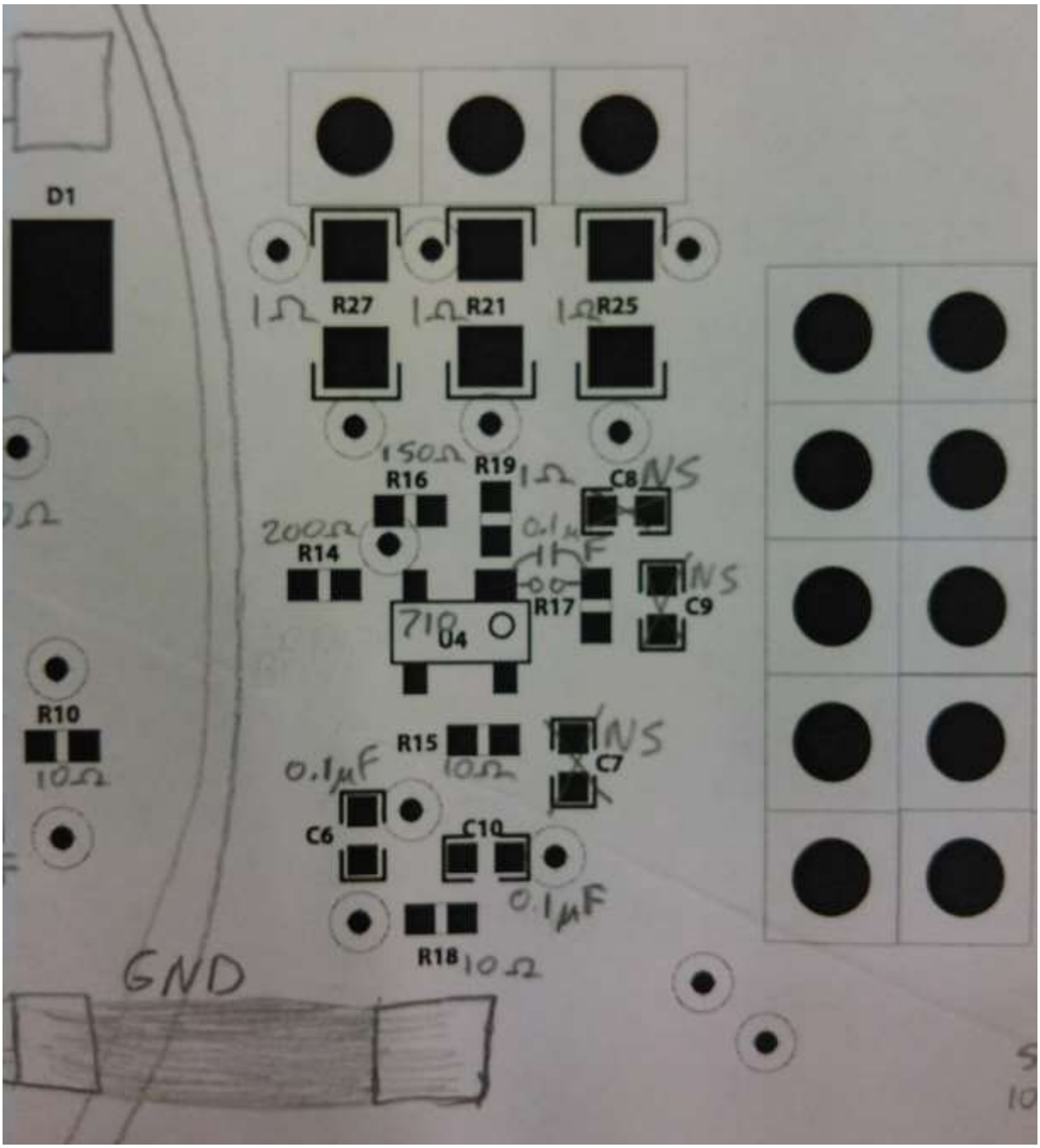
Running test bench.



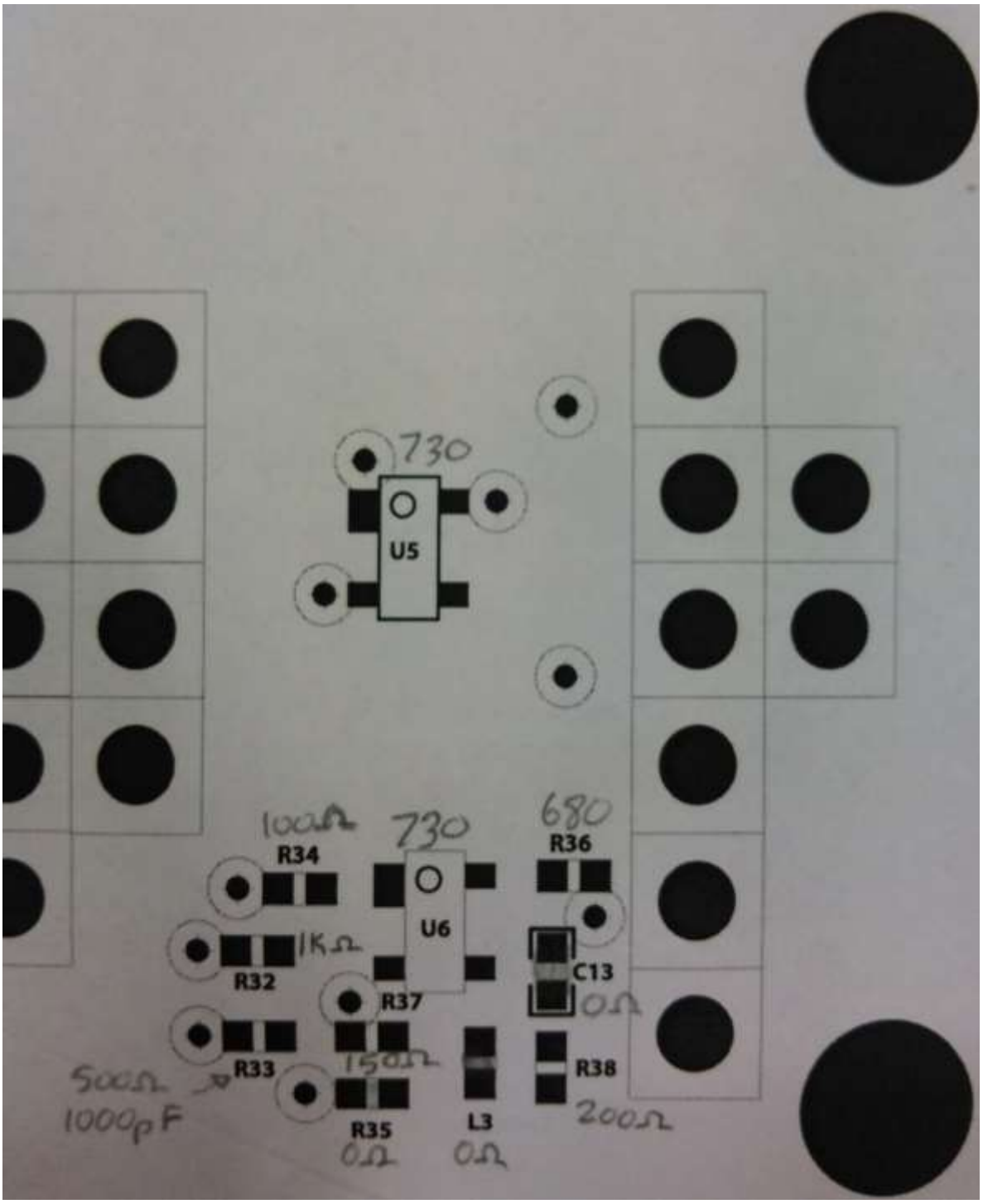
Stuffing for the board's top layer.



Values used on the first section of the board's top layer. Two diodes were used in series, instead of one, for D1.

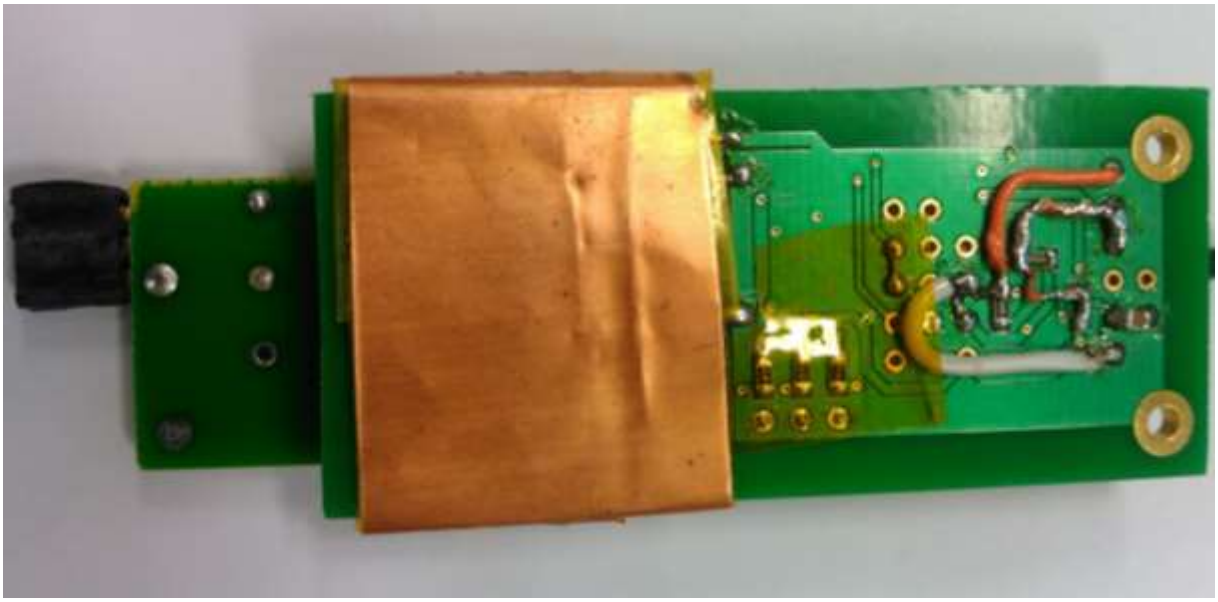


Values used on the mid-section of the board's top layer. U4 was changed to a 730, and R15 was changed to 33Ω.

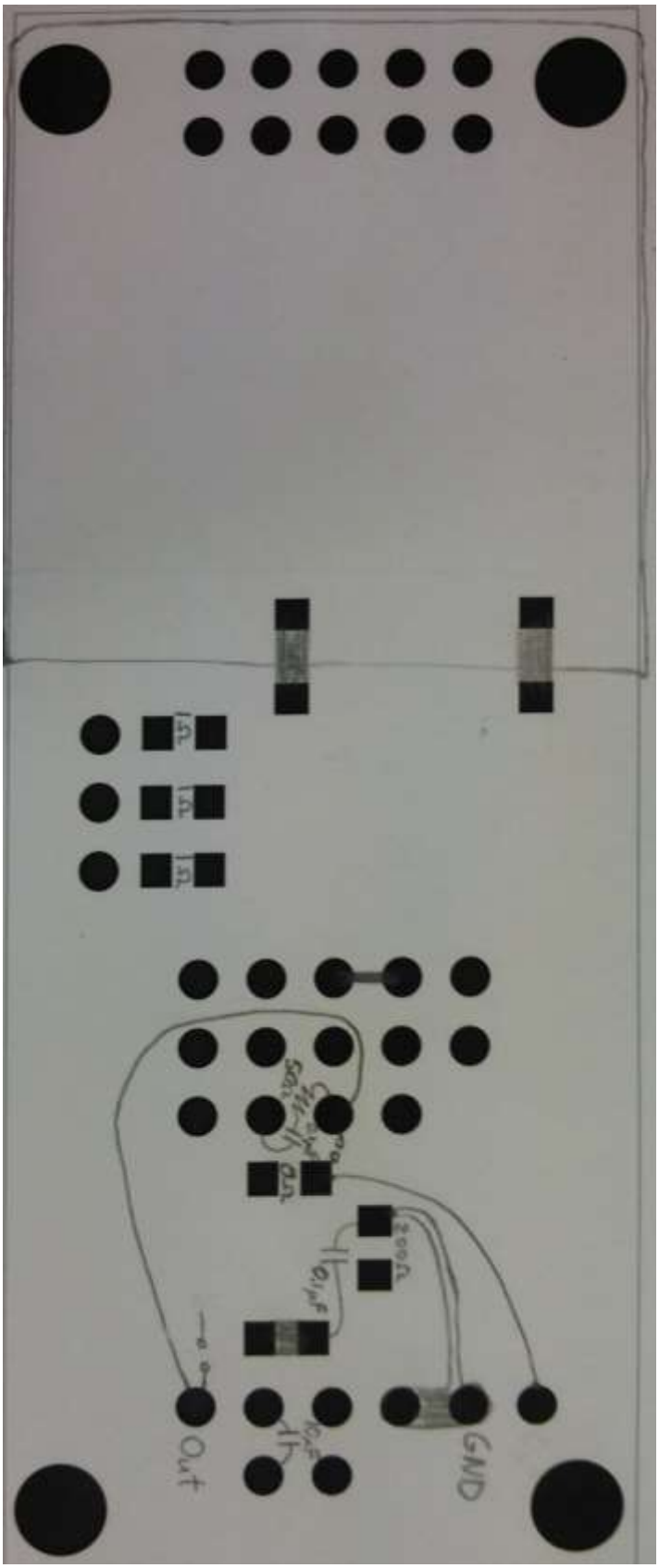


Values used on the output-section of the board's top layer. R34 was changed to 300Ω.

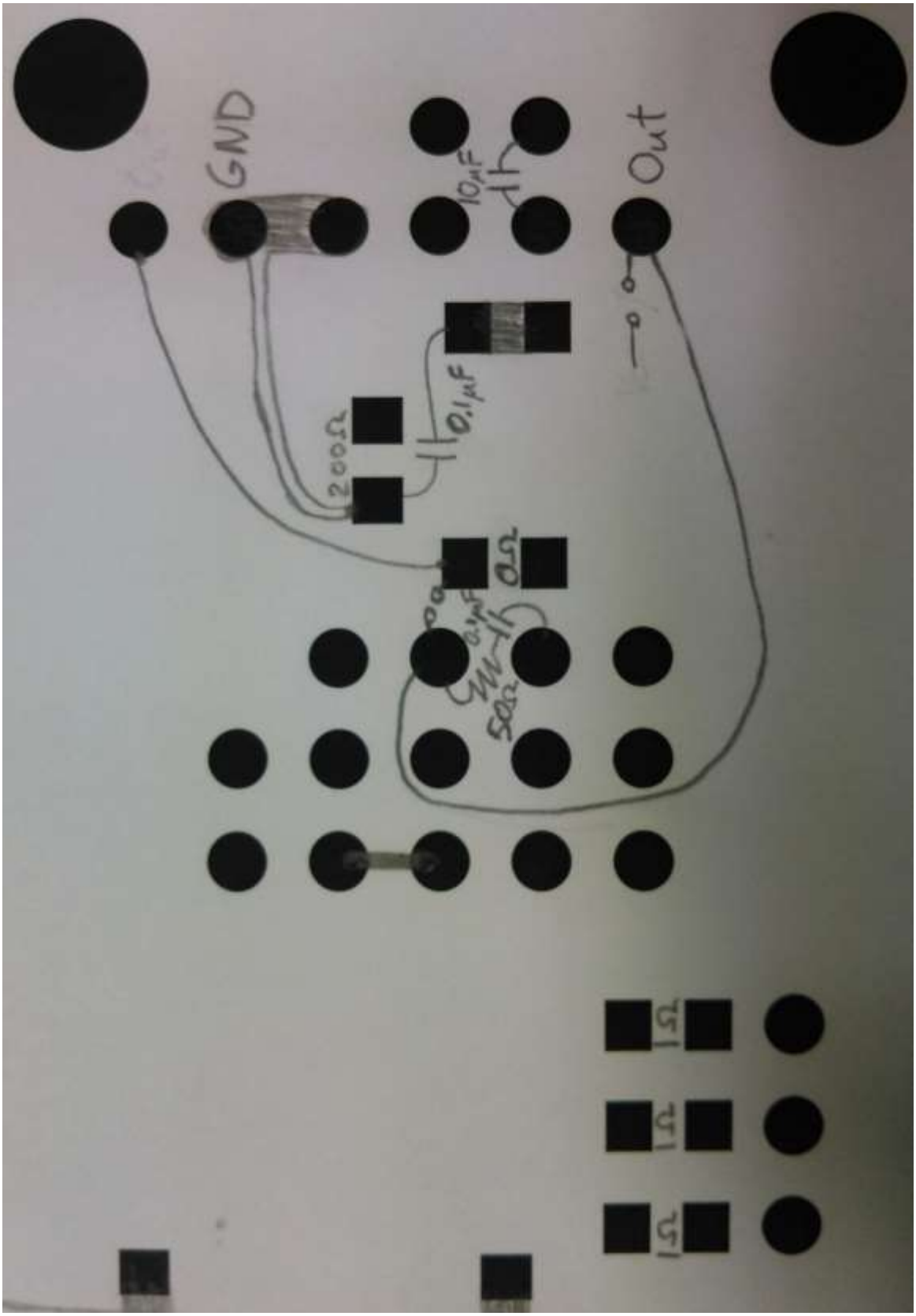
The bottom layer of the board looks like this:



Some copper braid was used to connect the ground side of the 200 Ω to the ground connector holes for better connection to ground on the output signal. The white wire is carrying the output signal to a hole that used to be VCC, but the trace to VCC was cut in order to use this as the output for the signal. One of the resistor pads were bridged together with solder and a small piece of wire to create a more direct connection to ground at that node. The same was done for the 0Ω resistors that used to connect the ground from one side of the board to the other. The trace seen on the board at the top of this image is soldered together because it was previously cut while experimenting with the circuit and looking for better ways of cleaning the signal. The large copper shields the bottom side of the board and is soldered on to the ground of the board's top layer. The side of the copper shield that is towards the board is covered in Kapton tape, as well as the whole bottom of the board, to avoid shorting to ground when pressed on.



Stuffing for the board's bottom layer.



Values used on the board's bottom layer.

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The following are sample signals while using Cesium-137 as a source. The inputs to the board include a 4V supply, an 8V supply, and a -1.75kV supply.

- Peak time: 1.48 ns
- Peak voltage: 234 mV

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- Peak time: 1.32 ns
- Peak voltage: 230 mV

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- Peak time: 1.44 ns
- Peak voltage: 212 mV

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- Peak time: 1.32 ns
- Peak voltage: 222 mV

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- Peak time: 1.32 ns
- Peak voltage: 234 mV

- Peak time: 1.32 ns
- Peak voltage: 209 mV

- Peak time: 1.40 ns
- Peak voltage: 209 mV

- Peak time: 1.40 ns
- Peak voltage: 216 mV

- Peak time: 1.40 ns
- Peak voltage: 207 mV

- Peak time: 1.48 ns
- Peak voltage: 193 mV

- Peak time: 1.08 ns
- Peak voltage: 239 mV

This signal was the fastest one observed.

- Peak time: 1.08 ns
- Peak voltage: 239 mV

This is still the same signal as the previous one. This shows that the signal lasted 3.2 ns, and reached steady state within 10ns from the moment the signal was received.

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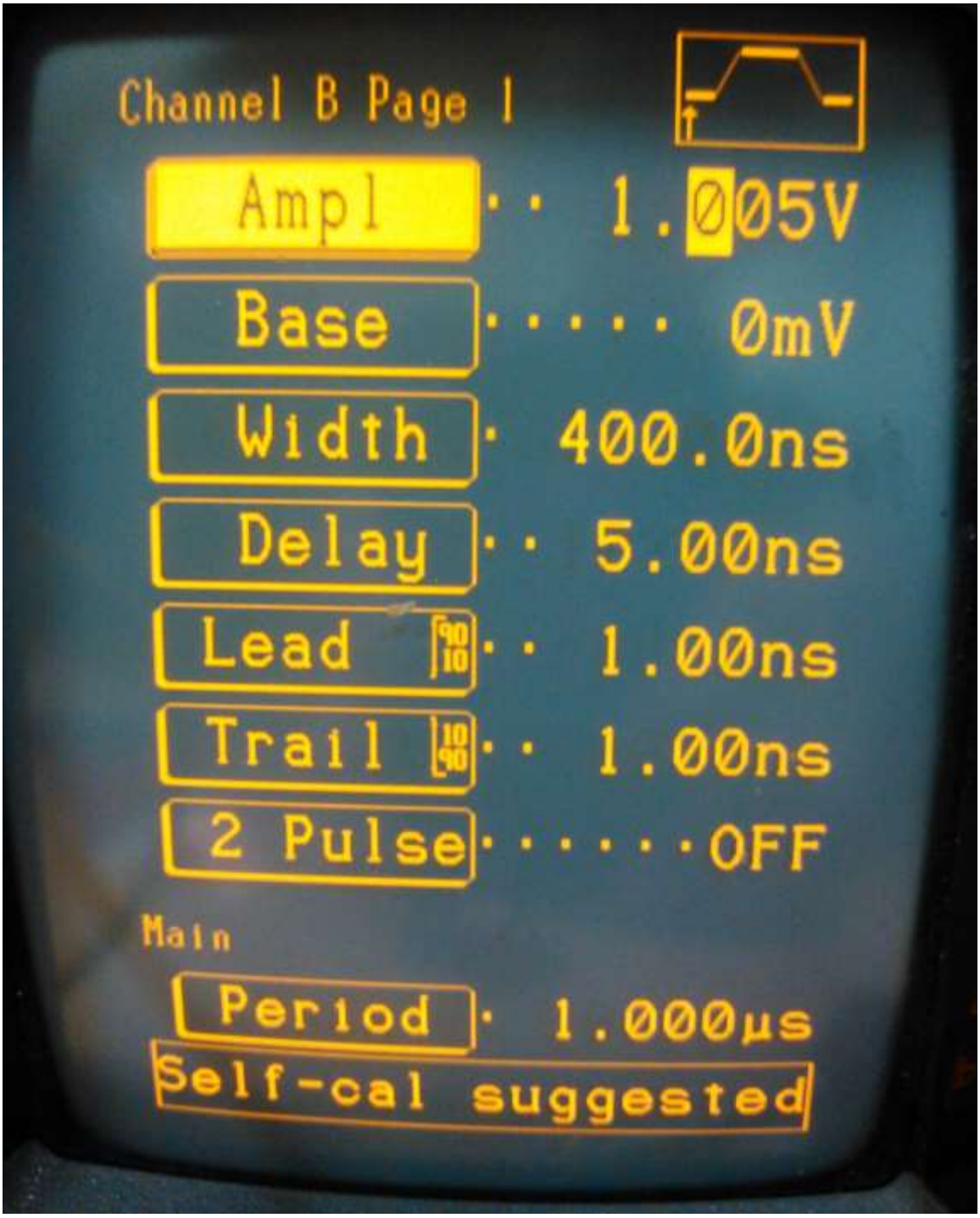
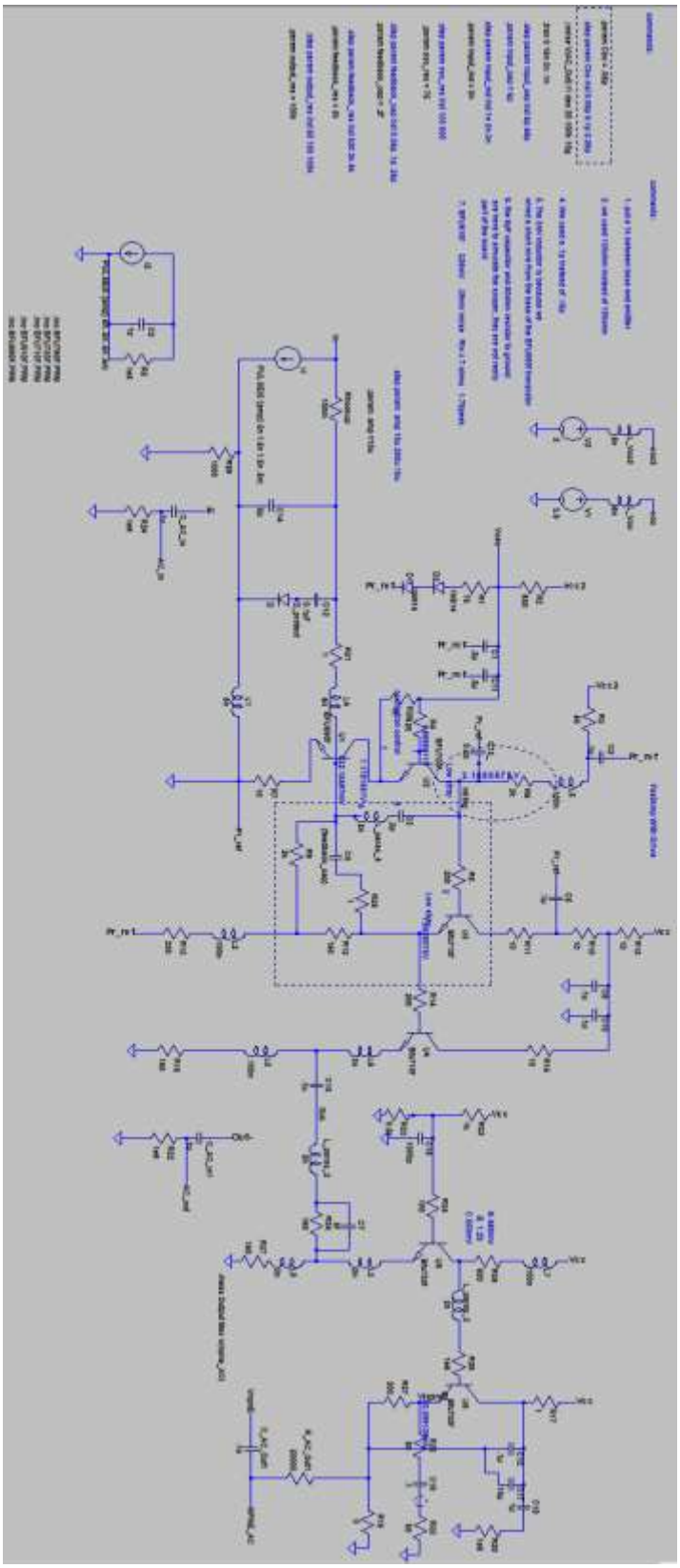
This odd signal ocurred during the beginning of testing. In the beginning, a few signals were giving positive peak, but this one has the largest peak voltage and shows that at around -270mV is the limit for the negative peak.



These are the settings on the pulse generator when it was being used as the input signal for the board.



LT Spice Schematic for Board 1