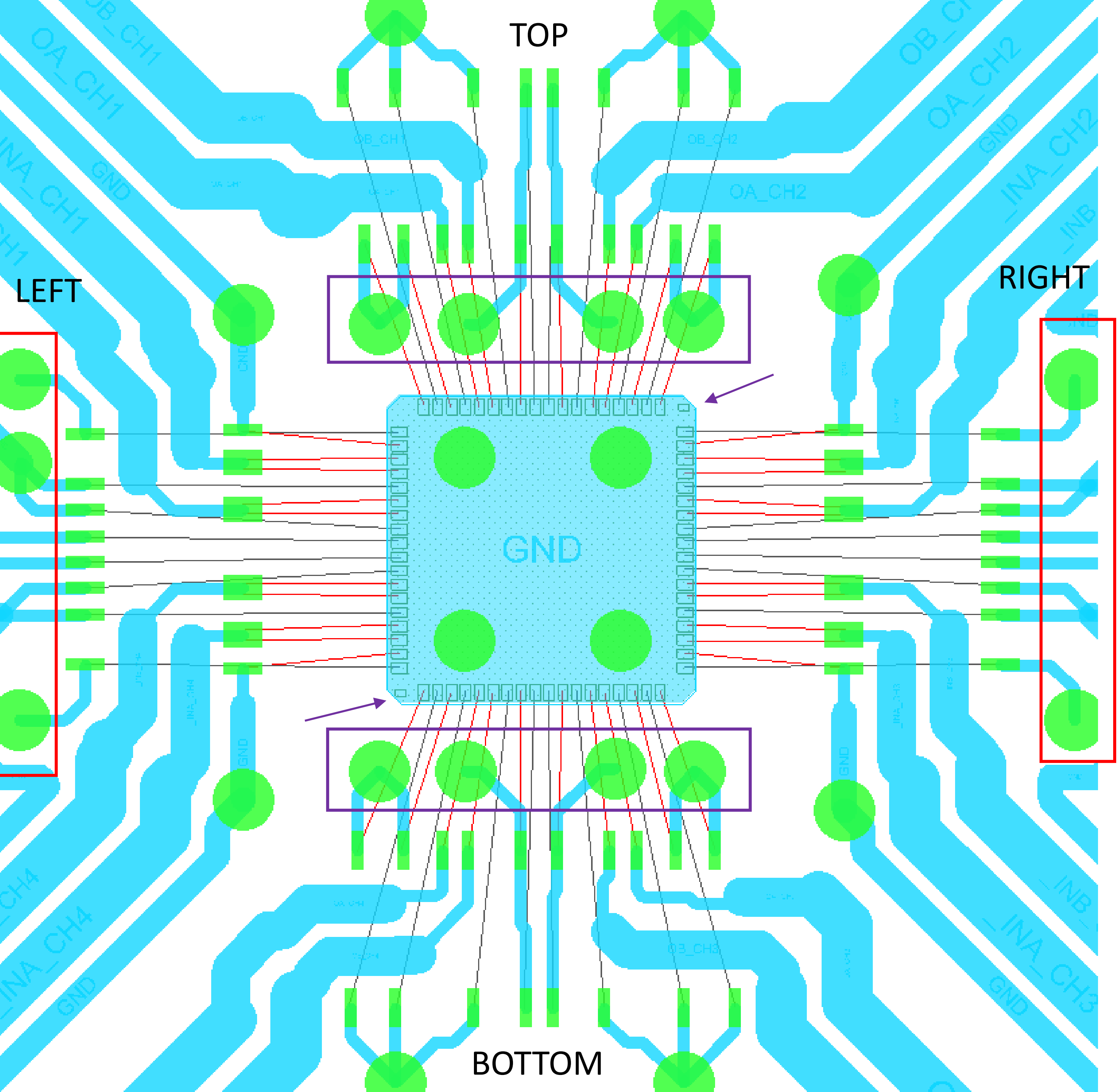
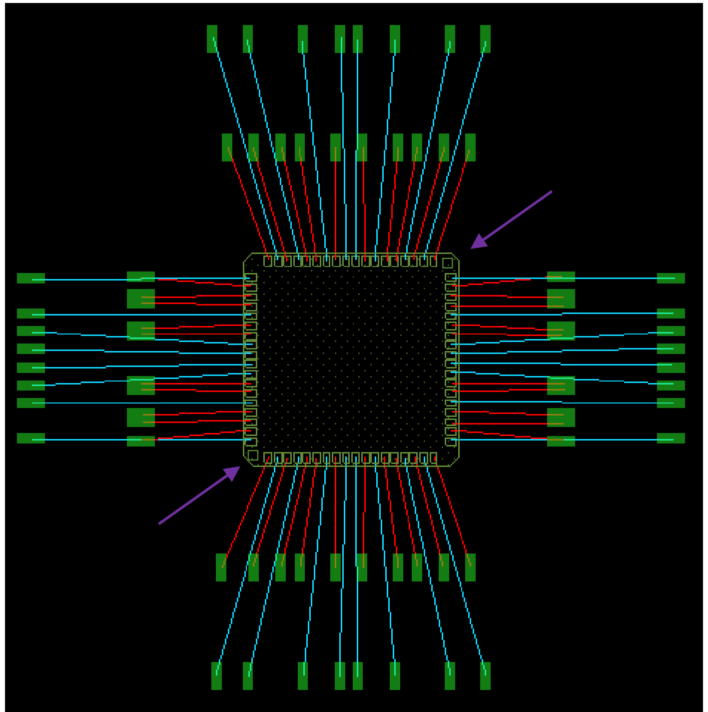
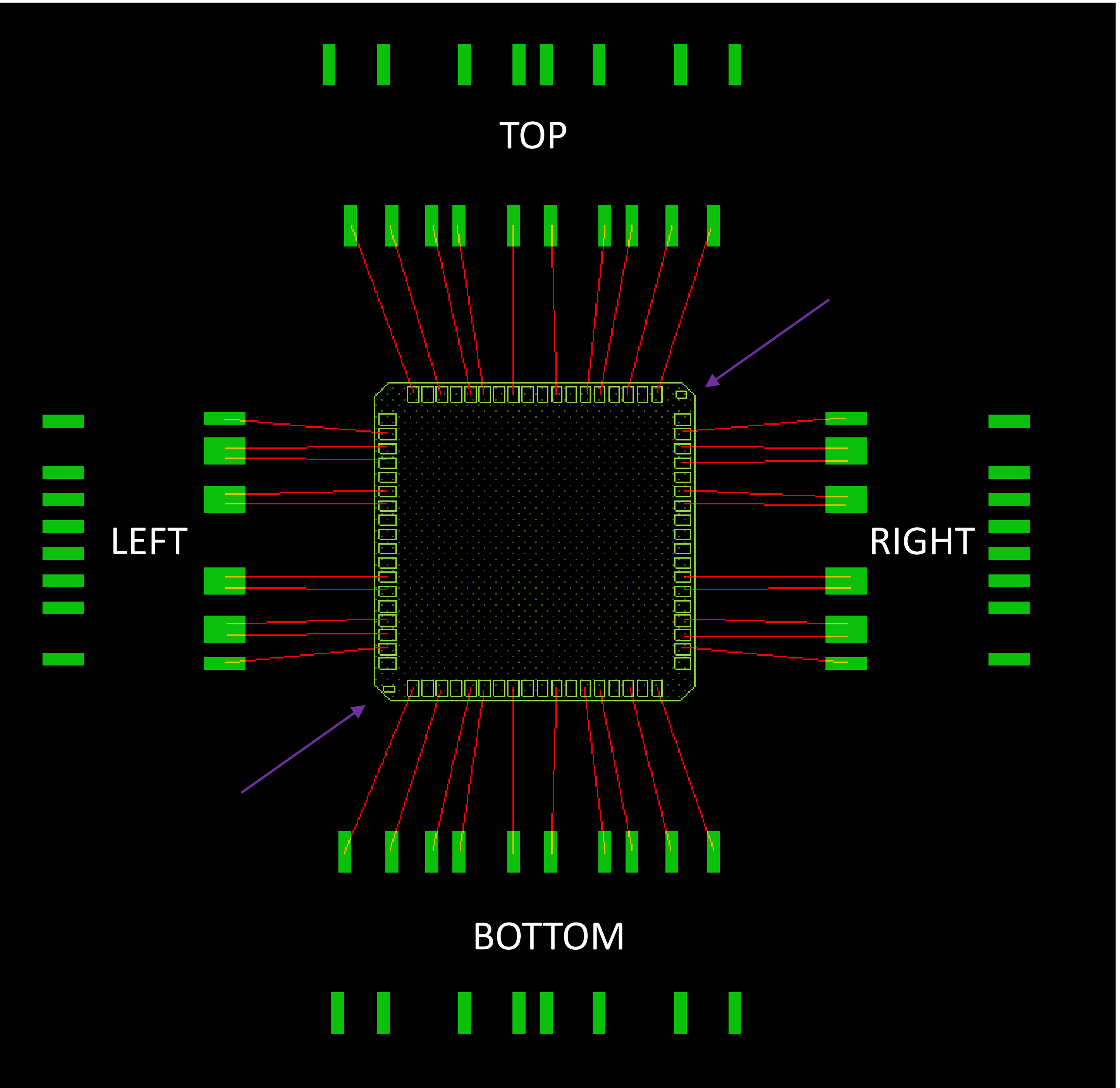


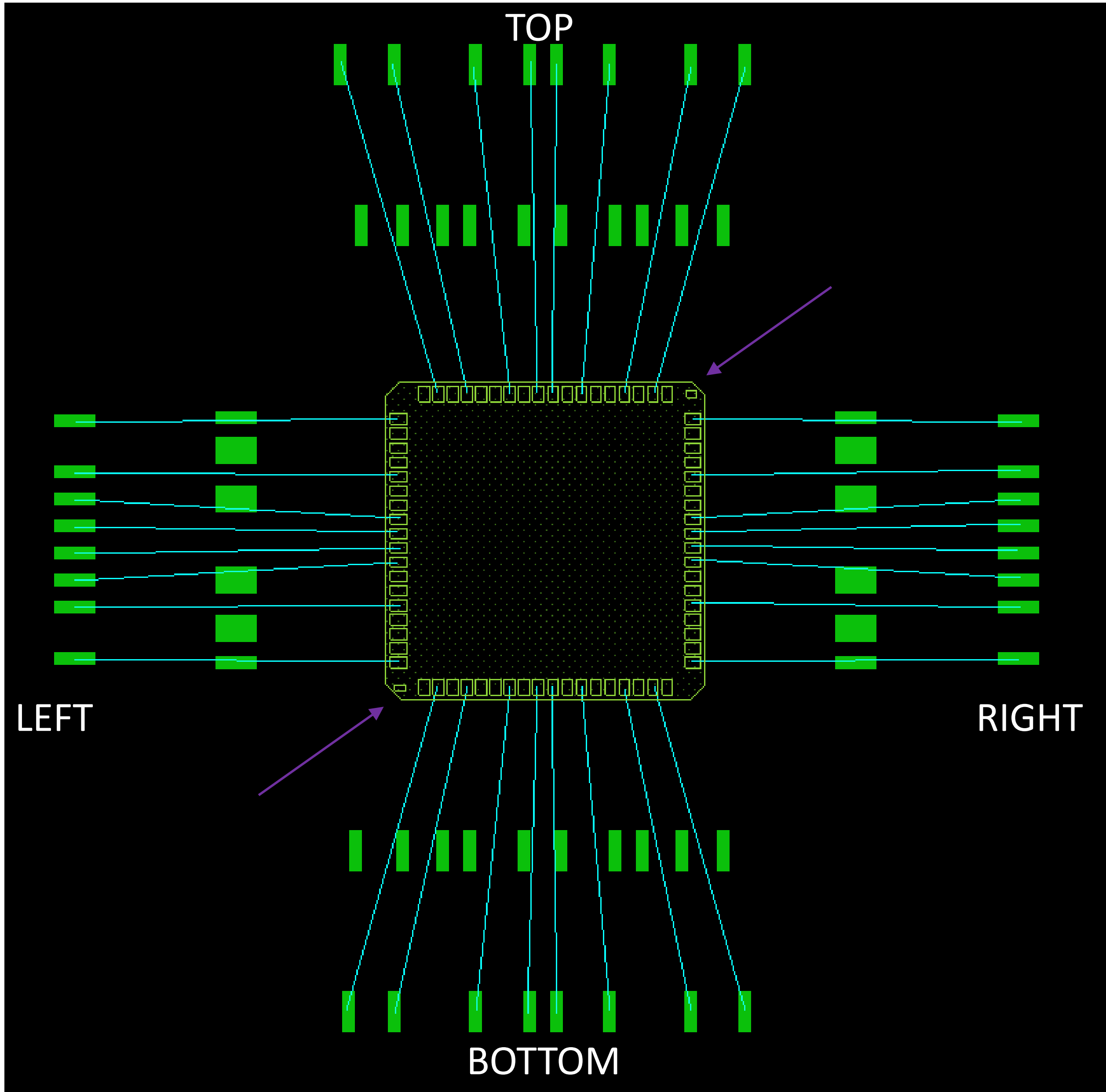
First the board is oriented with the component-side upwards. Then board must be oriented so that the set of four vias, denoted by the purple boxes, are on the top and bottom edges. The chip must be aligned with the board so that the two tabs on opposite corners of the chip are on the top right and bottom left of the chip, as denoted by the purple arrows. The chip is not symmetric about the vertical and horizontal axes, so there is a distinction between the top and bottom. The left side of the board is denoted by three vias that line up (see red boxes) while on the right side only two vias line up by the outer layer of pads.

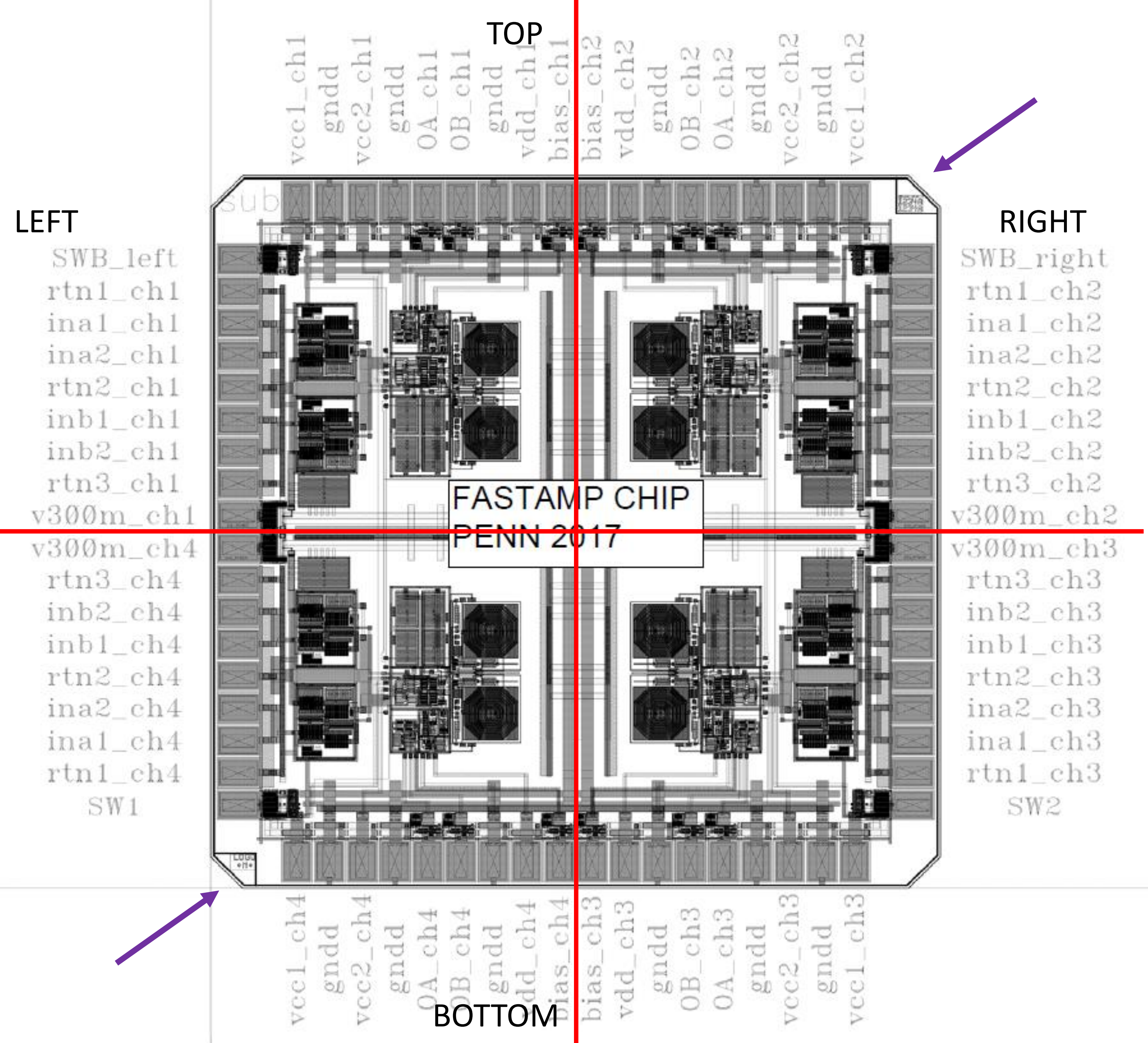
The second picture is a simplified view of the chip and pads to emphasize the wire bonding pattern. Note the tabs in the top-right and bottom-left signify the orientation of the chip relative to the bond pads, as in the diagram to the left.



Wire Bond Diagrams depicting the inner layer bond pad wirings to the left, and the outer layer bond pad wirings to the right.






TOP
vcc1_ch1
gndd
vcc2_ch1
gndd
OA_ch1
OB_ch1
gndd
vdd_ch1
bias_ch1
bias_ch2
vdd_ch2
gndd
OB_ch2
OA_ch2
gndd
vcc2_ch2
gndd
vcc1_ch2
LEFT
SWB_left
rtn1_ch1
ina1_ch1
ina2_ch1
rtn2_ch1
inb1_ch1
inb2_ch1
rtn3_ch1
v300m_ch1
v300m_ch4
rtn3_ch4
inb2_ch4
inb1_ch4
rtn2_ch4
ina2_ch4
ina1_ch4
rtn1_ch4
SW1
RIGHT
SWB_right
rtn1_ch2
ina1_ch2
ina2_ch2
rtn2_ch2
inb1_ch2
inb2_ch2
rtn3_ch2
v300m_ch2
v300m_ch3
rtn3_ch3
inb2_ch3
inb1_ch3
rtn2_ch3
ina2_ch3
ina1_ch3
rtn1_ch3
SW2
sub
FASTAMP CHIP
PENN 2017
vcc1_ch4
gndd
vcc2_ch4
gndd
OA_ch4
OB_ch4
gndd
vdd_ch4
bias_ch4
bias_ch3
vdd_ch3
gndd
OB_ch3
OA_ch3
gndd
vcc2_ch3
gndd
vcc1_ch3
BOTTOM