Penn SBIR II Hyperfast Silicon Sub-Contract Participation Narritive

Summer 2019 Provide two four channel Fast Amp boards for tests with 2X2 screened APD arrays then redesign the original Fast Amp 4 channel board to be mechanically compatible with a nearly edge-less integration of the inner borders of 4 APD sensors. Assemble and test these boards after fab at a commercial vendor and ASIC bonding at Princeton. This board will improve on the existing design with a better output signal hookup and provide external access to the 5X gain switch and other optional configuration modes. Manny Morales, Mitch Newcomer

Fall 2019 The Fast Amp circuit was fabbed in Global Foundries 180nm Silicon Germanium Process to allow a high speed APD readout to be explored and tested. This process is not suitable for integration of the front end signal processing with the complex digital logic that will be required to digitize the output data (time and charge) information in a high channel count detector system needed for operation in the HL LHC or future collider experiments. It is also not sufficiently radiation tolerant for long term operation at high eta within a few meters of the interaction point. For this reason we will turn our attention the next stage of readout development to TSMC's 65nm process that Penn has access to through signed NDA's with TSMC through CERN and IMEC brokered agreements. This process has been chosen by several detector sub systems including the CMS and ATAS Pixel detectors for it high radiation tolerance, high quality analog models, access to digital library cells. Studies by the combined AMS and ATALS RD53 collaboration resulted in their choice of this technology for operation in the highest radiation environment in their respective detector systems. We will examine front end circuit configurations under development in CMOS for use in ATLAS HGTD timing layer (130nm CMOS) and in CMS's End cap timing layer (65nm CMOS) for precision timing and call on our experience with the screened APD readout using a fast bipolar process. In order not to get bogged down in the development of a sophisticated digital back end at this stage we will send out two signals from each APD channel to an external DAQ system. A fast analog pulse with a one to two nanosecond peaking time and a pulse whose front edge is determined by a low threshold leading edge discriminator and whose back end is strongly correlated to the zero crossing time of a bipolar version of the APD signal. Utilizing the two timing edges and an analog representation of the size of the initial part of the APD pulse we should be able to establish an excellent time resolution.

Design and development of a 4 channel CMOS precision timing ASIC in TSMC's 65nm process.

Winter 2019 – 2020 Front end CMOS followed by comparator and zero crossing circuit design and development MSEE with guidance from Mitch Newcomer

Spring 2020

- Layout of single channel circuit, chip level services. MSEE with guidance from Mitch Newcomer
- Chip footprint pad definitions placement, power nets, block placement Nandor Dressnandt Initial P&R of 4 channel blocks Nandor Dressnandt with assistance from MSEE

Summer 2020

- Complete P&R Nandor Dressnandt
- Extracted NL simulations MSEE, Mitch Newcomer, Nandor

- Submit ASIC for Fab August 2020
- Submit Sub-contractor section of Year 1 progress report

Fall 2020

- Design 2X2 board for four channel Precision Timing ASIC Manny Morales
- Receive boards from Fab assemble solder mountable components
- Send to Princeton for bonding CMOS ASIC
- Bench testing of 2X2 Precision Timing board
- Source testing with APD ASICs. Send to other institution for tests with beam

Winter 2020 -21

- Design 4X4 Array board with 4 CMOS precision timing ASICs to read out 16 APD's
- Fab and Assemble boards Send out for bonding of ASICs
- Receive Boards with bonded ASICs perform and characterize

Spring 2021

- Assemble & test 15 additional 4X4 boards for multi – plane beam tests.

Summer 2021

- Summarize Test Results plan for next stage of development
- Write/submit up SBIR II progress report