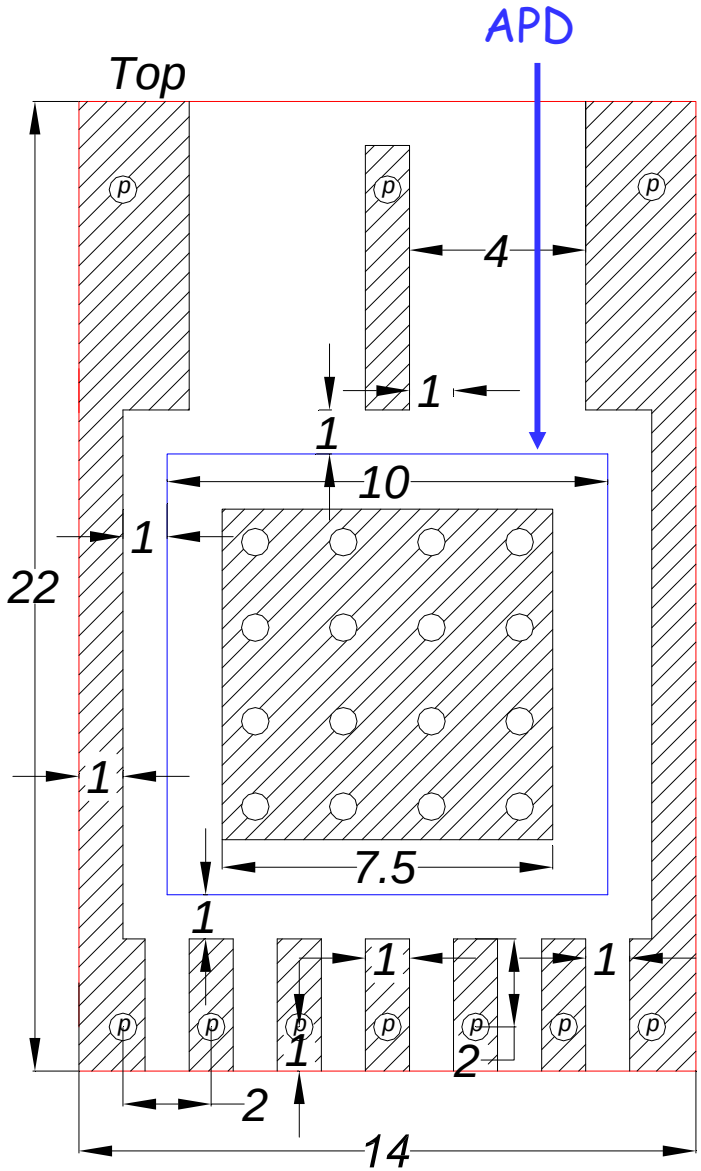
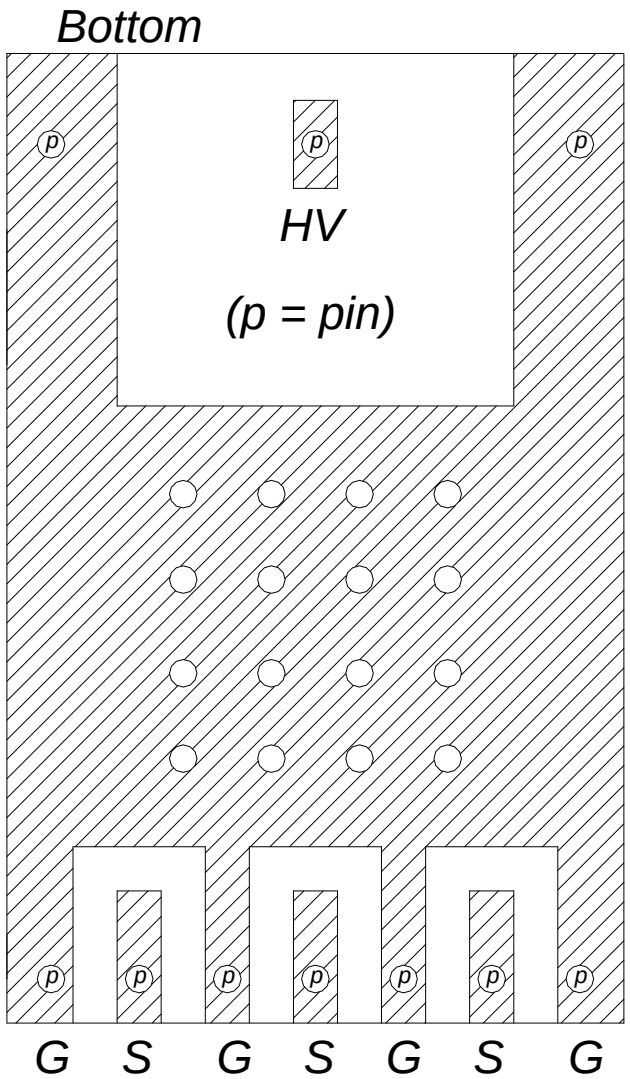
G10 Carrier Board for RMD 8x8 mm^2 APDs

B. Harrop, K. McDonald, M. Newcomer

Apr. 6, 2017

First try at a layout, 3/22/17:





G10 carrier board is 14x22 mm^2.

APDs have 10x10 mm^2 total area, mounted on the top of the carrier board.

APD bottom contact is 7.5x7.5 mm^2.

All vias are plated thru, and have pins, soldered on the bottom side.

Wire bonds connect the HV and S (signal) solder pads to the APD.

The HV pad, and the HV wire bond, are encased in conformal coating, on both top and bottom of the carrier board.

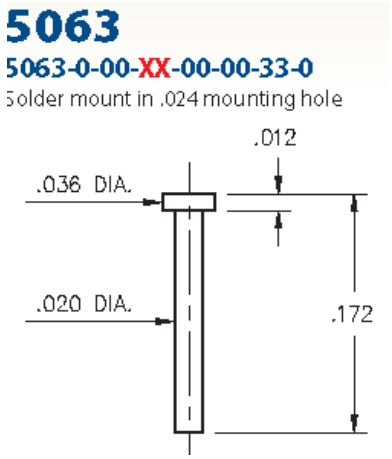
Pins and Sockets

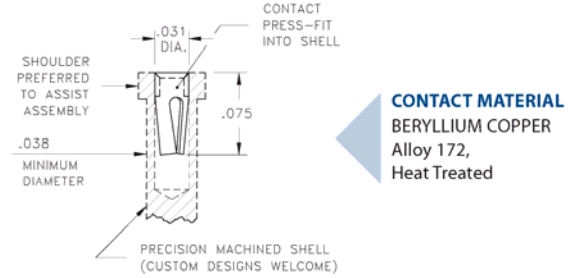
Better to have sockets on the carrier board, pins on the preamp board. (Repair of a pin easier on a board without an APD.)

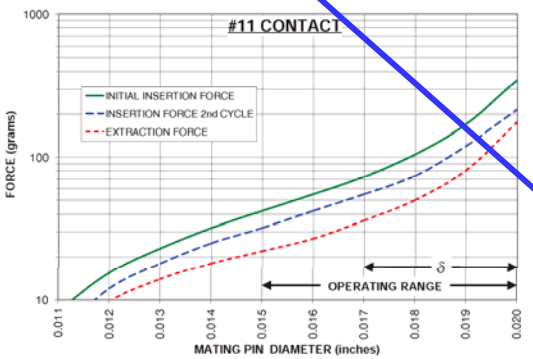
Pins could be Mill-Max 5063-0-00-15-00-33-0 "nail head" type, 0.020" pin diameter.
https://www.mill-max.com/assets/new_products/PCB%20Pins.pdf

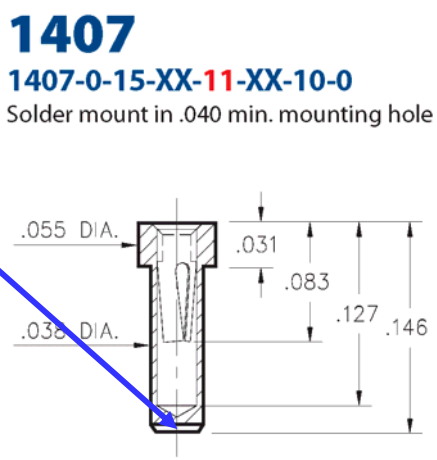
Sockets could be Mill-Max 1407-0-15-15-11-27-10-0, mounted with the pin hole on the bottom of the carrier board.
https://www.mill-max.com/assets/pdfs/153-201.pdf

Wire bonds will be made to the flat end of the socket.









SPECIFICATIONS:
Pin Material: Brass Alloy 360, 1/2 Hard (Except where noted)
Dimensions: Inches
Tolerances On: Lengths: ±.005 Diameters: ±.002 Angles: ±2°
RoHS-2 2011/65/EU

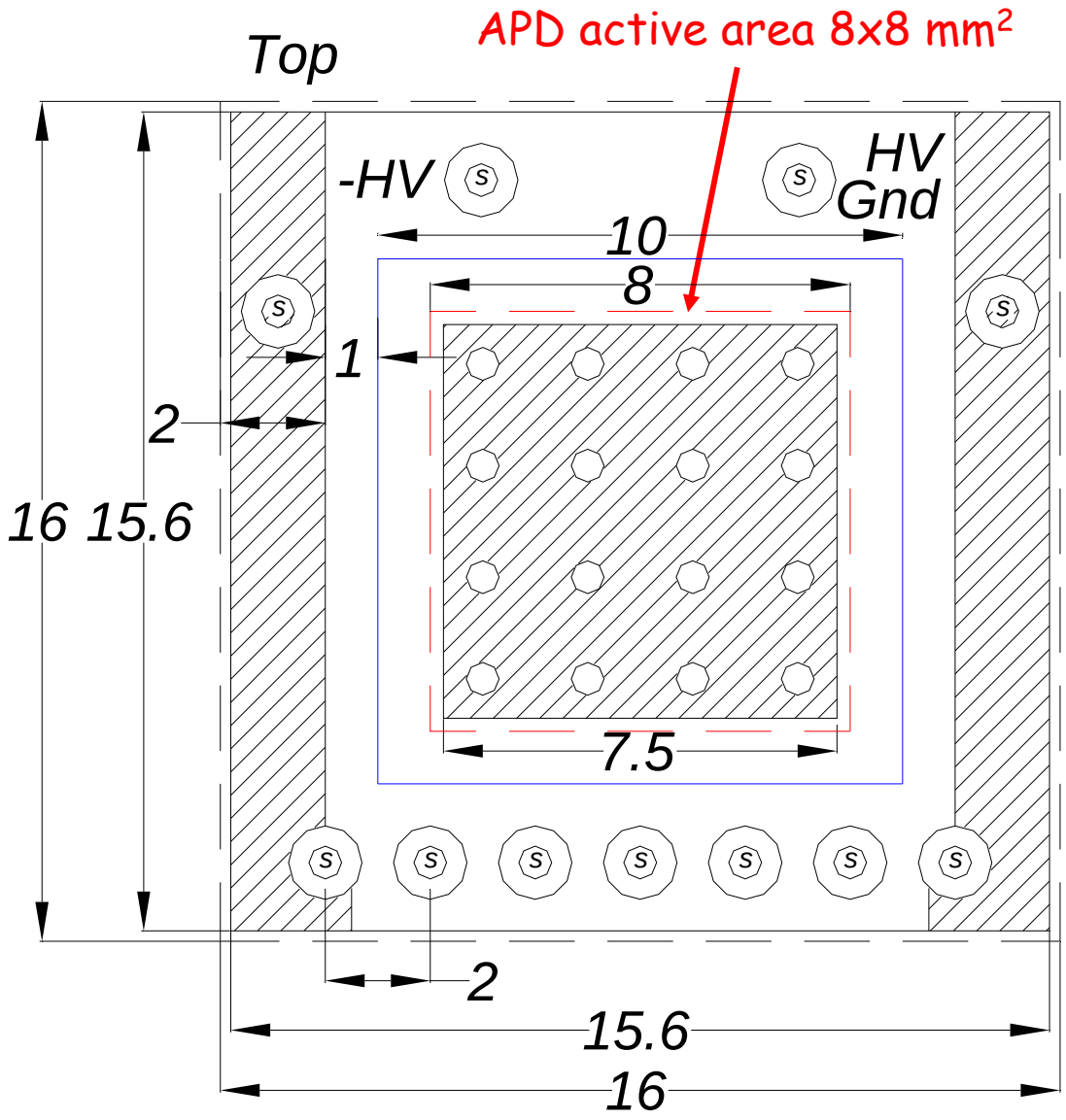
ORDER CODE: XXXX - X - 00 - XX - 00 - 00 - XX - 0
BASIC PART #
SPECIFY PIN FINISH:
01 200 µ" TIN/LEAD OVER NICKEL
◆ **80** 200 µ" TIN OVER NICKEL (RoHS)
◆ **15** 10 µ" GOLD OVER NICKEL (RoHS)
◆ **21** 20 µ" GOLD OVER NICKEL (RoHS)
◆ **34** 50 µ" GOLD OVER NICKEL (RoHS)

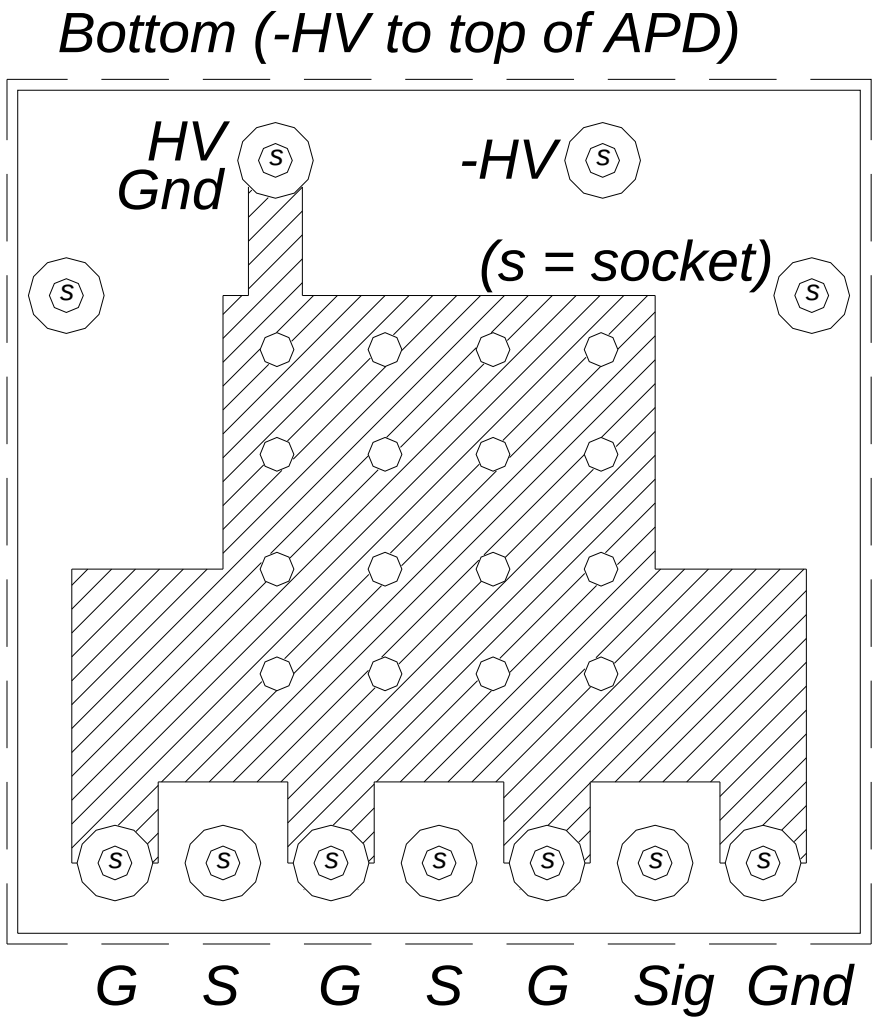
SPECIFICATIONS:
Shell Material: Brass Alloy 360, 1/2 Hard
Contact Material: Beryllium Copper Alloy 172, HT
Dimensions: Inches
Tolerances On: Lengths: ±.005 Diameters: ±.002 Angles: ±2°
RoHS-2 2011/65/EU

ORDER CODE: XXXX - X - XX - XX - XX - XX - XX - 0
BASIC PART #
SPECIFY SHELL FINISH:
01 200 µ" TIN/LEAD OVER NICKEL
◆ **80** 200 µ" TIN OVER NICKEL (RoHS)
◆ **15** 10 µ" GOLD OVER NICKEL (RoHS)
SPECIFY CONTACT FINISH:
02 100 µ" TIN/LEAD OVER NICKEL
◆ **84** 100 µ" TIN OVER NICKEL (RoHS)
◆ **27** 30 µ" GOLD OVER NICKEL (RoHS)
SELECT CONTACT:
#11 or #21 CONTACT (DATA ON PAGE 251)
(For alternate contact choices, see group A on page 248)

Carrier Board Sized for Tiling

The active area of an APD is 8x8 mm^2.
So, to make a square tiling of such APDs, they could be on a carrier board that is 16x16 mm^2, with 25% active area per layer of tiling, and 4 tiling layers for 100% active area.
The carrier board is actually 15.6 x 15.6 mm^2, with the APD mounted on its top.



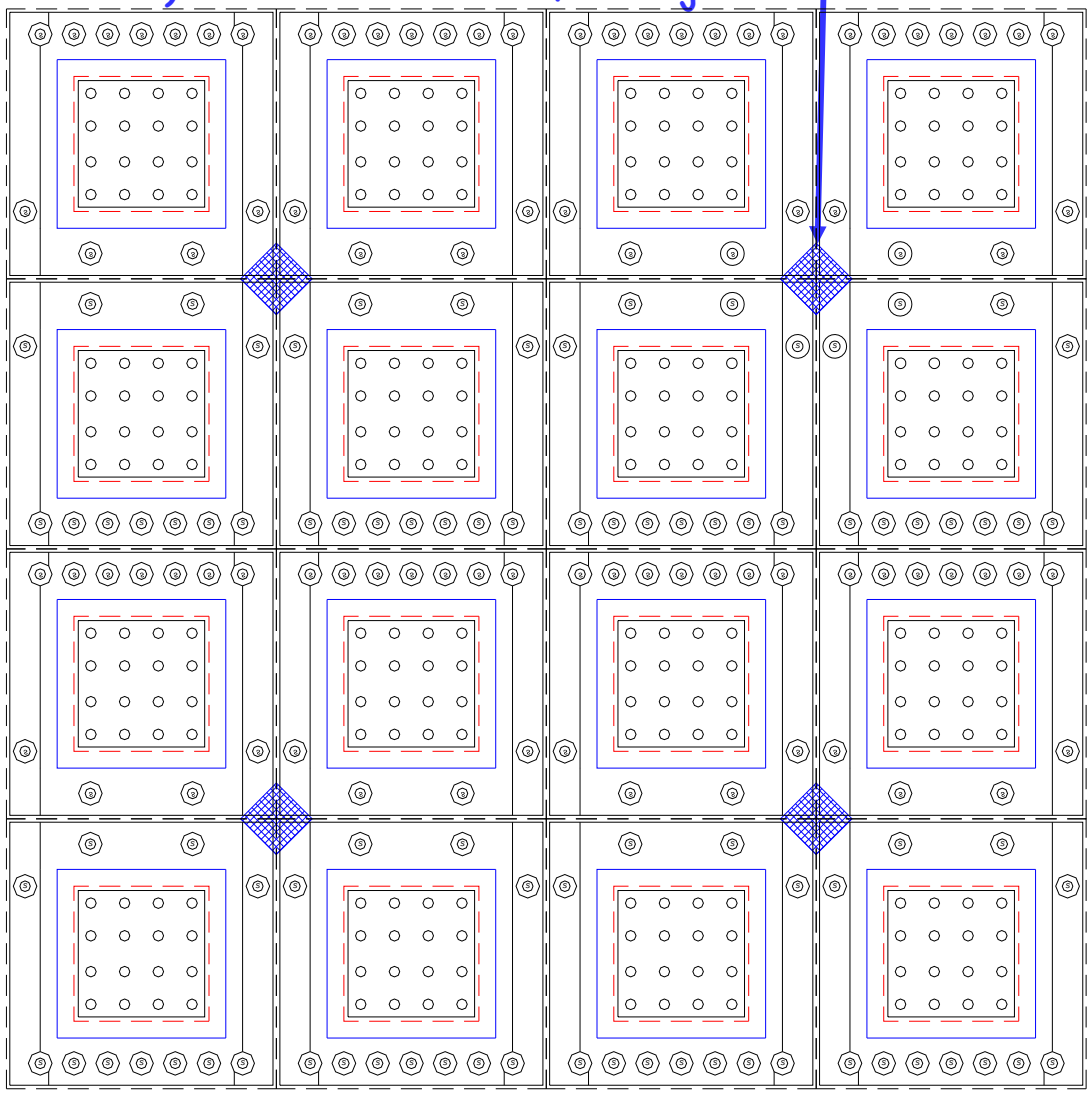


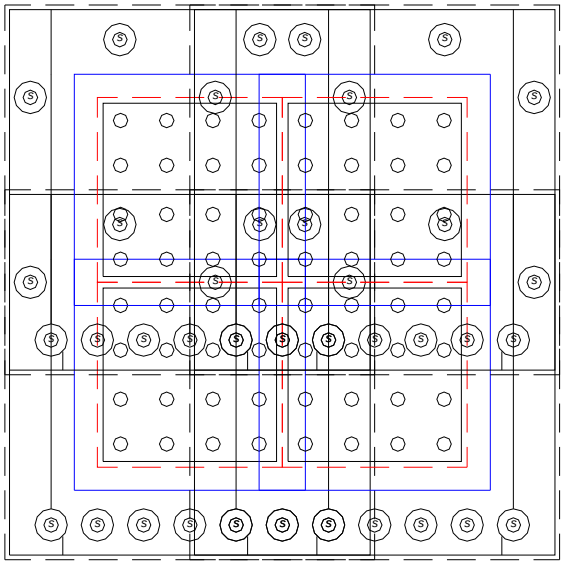
Tiling, II

4 tiling layers, with offsets of 8 mm, achieve 100% coverage.

Example of a single tile layer of 4 x 4 carrier boards.

The eventual 4-ch Penn preamp ASIC will be 3x3 mm^2 (shown in blue below), and would be located (on a large readout board) at the corners of 4 adjacent carrier boards.

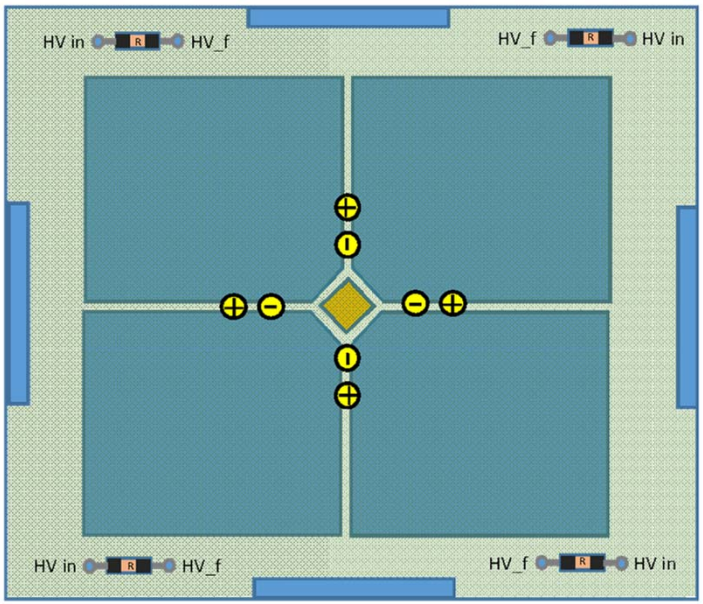




Back View (back of PCB)

Readout/HV/PWR

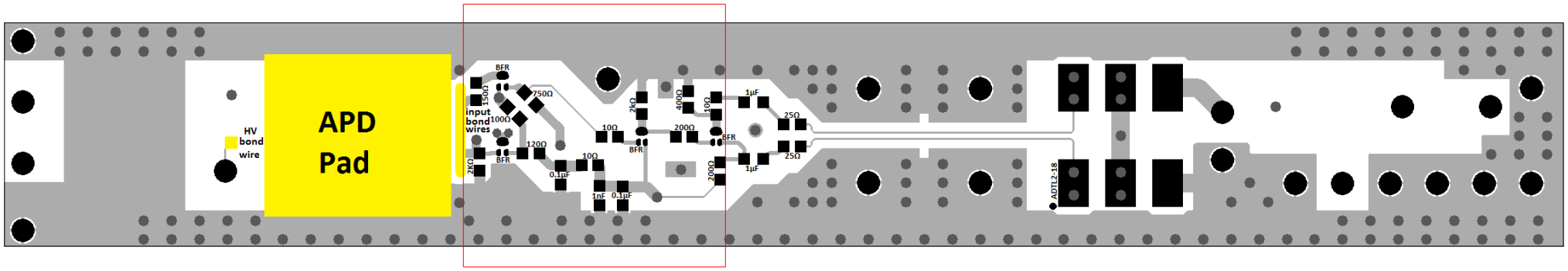
Amplifier Signal Routed out on back



The next iteration of the surface-mount Penn preamps could be laid in a similar array.

Next Surface-Mount Preamp

The present Penn preamp is shown below, together with an indication of the 16x16 mm^2 footprint of the proposed carrier board.



16x16 mm^2 footprint of proposed carrier board

The surface-mount components of the preamp should be rearranged to fit within this footprint on bottom side of the preamp board, with the HV connection (and the sockets for the pins of the carrier board) on the top side.

The low-voltage power conditioning, and the signal and HV connectors, will be outside the footprint of the preamp itself, as on the present board. This items should be on the top side of the new preamp to facilitate stacking of the preamp + APD units into a relatively compact 4-layer detector.

The new preamp will include diode protection, and a test-pulse input.

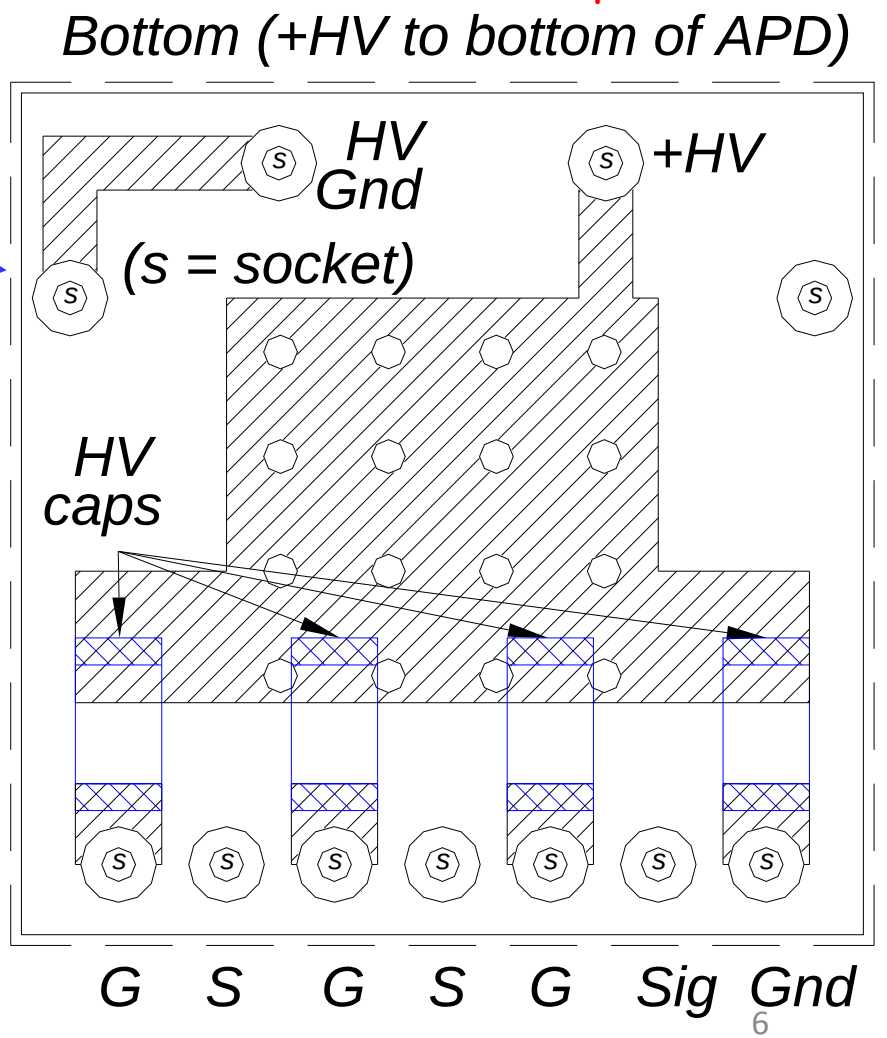
Option for +HV on the APD Bottom Side

The present scenario uses –HV on the top side of the APD, with the bottom side at ground.

Then, the mesh signal and the signal from the bottom side can both be read out directly, without coupling capacitors.

Alternatively, +HV could be applied to the bottom side of the APD, with the top side at ground.

Bottom of carrier board with +HV to the APD bottom side:



This requires that the signal from the bottom side be read out via coupling capacitors (Vishay VJ120-Y-500-M-X shown), which will slightly increase the signal rise time, ⇒ slightly worse time resolution.

The perceived advantage is that the mesh and the APD top are both at ground, which reduces risk of HV breakdown here.

As this seems to be a non-issue, we are NOT in favor of the +HV scenario.

Isochronous Signal Lines to the Penn ASIC

The Penn ASIC will collect the signals at one corner of the 16x16 mm^2 footprint of the tiled APD layout.

This gives us an opportunity to reduce the time walk by making the signal lines isochronous (equal length) from the "pins" along one edge of the footprint over to the input pad of the ASIC.