G10 Carrier Board for RMD 8x8 mm^2 APDs

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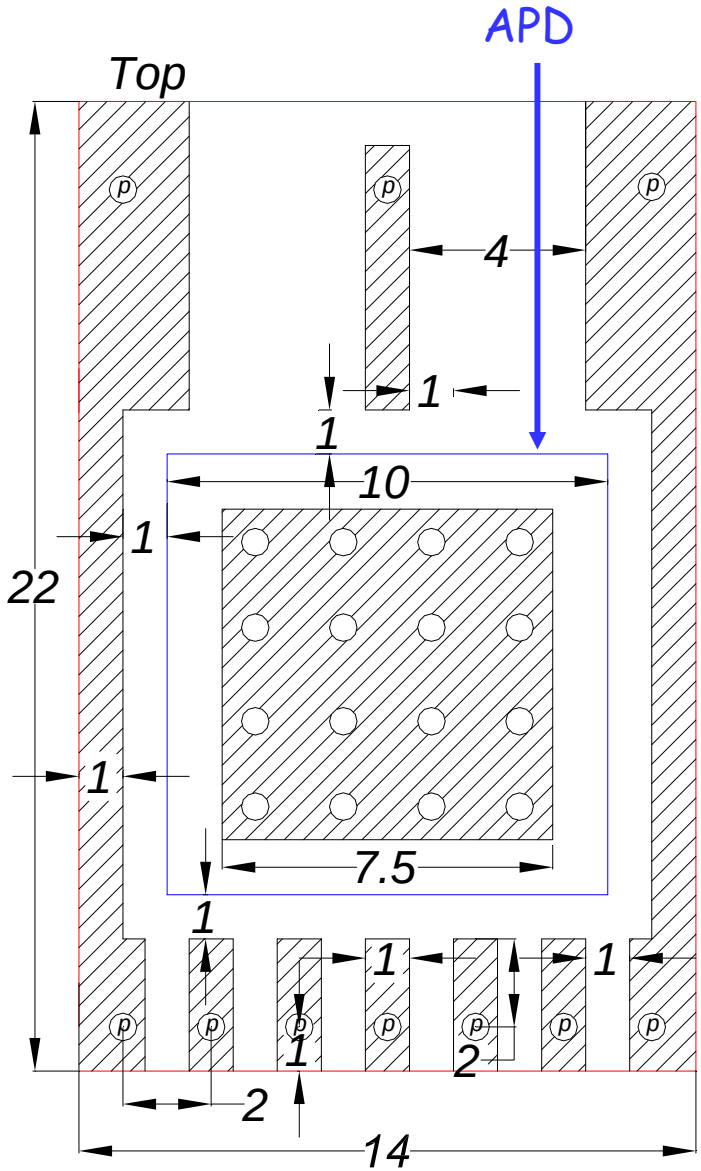
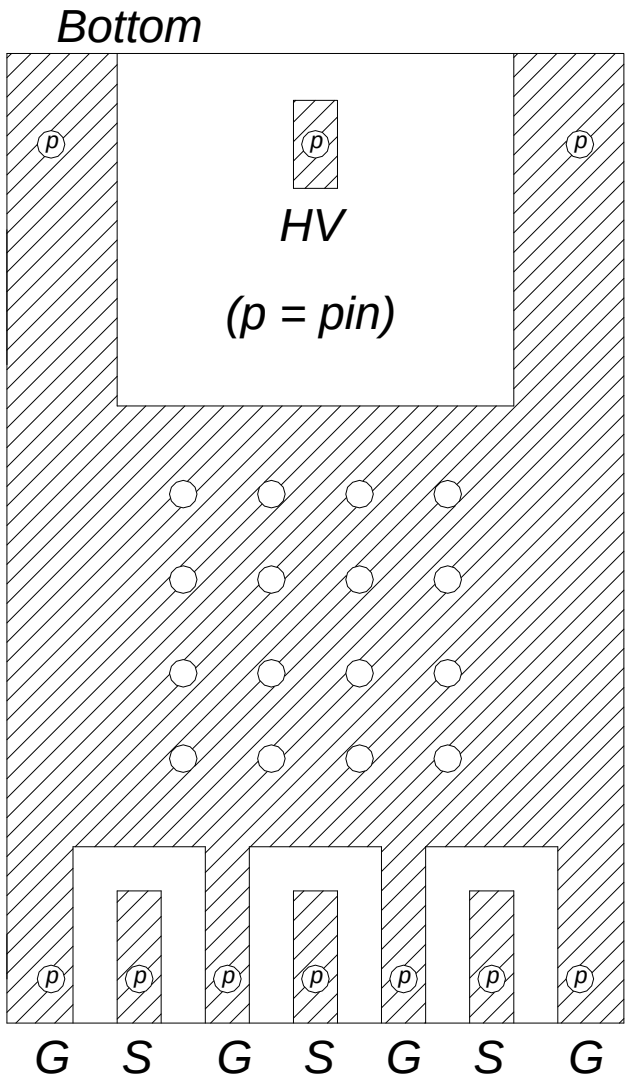
First try at a layout, 3/22/17:





G10 carrier board is 14x22 mm^2.

APDs have 10x10 mm^2 total area, mounted on the top of the carrier board.

APD bottom contact is 7.5x7.5 mm^2.

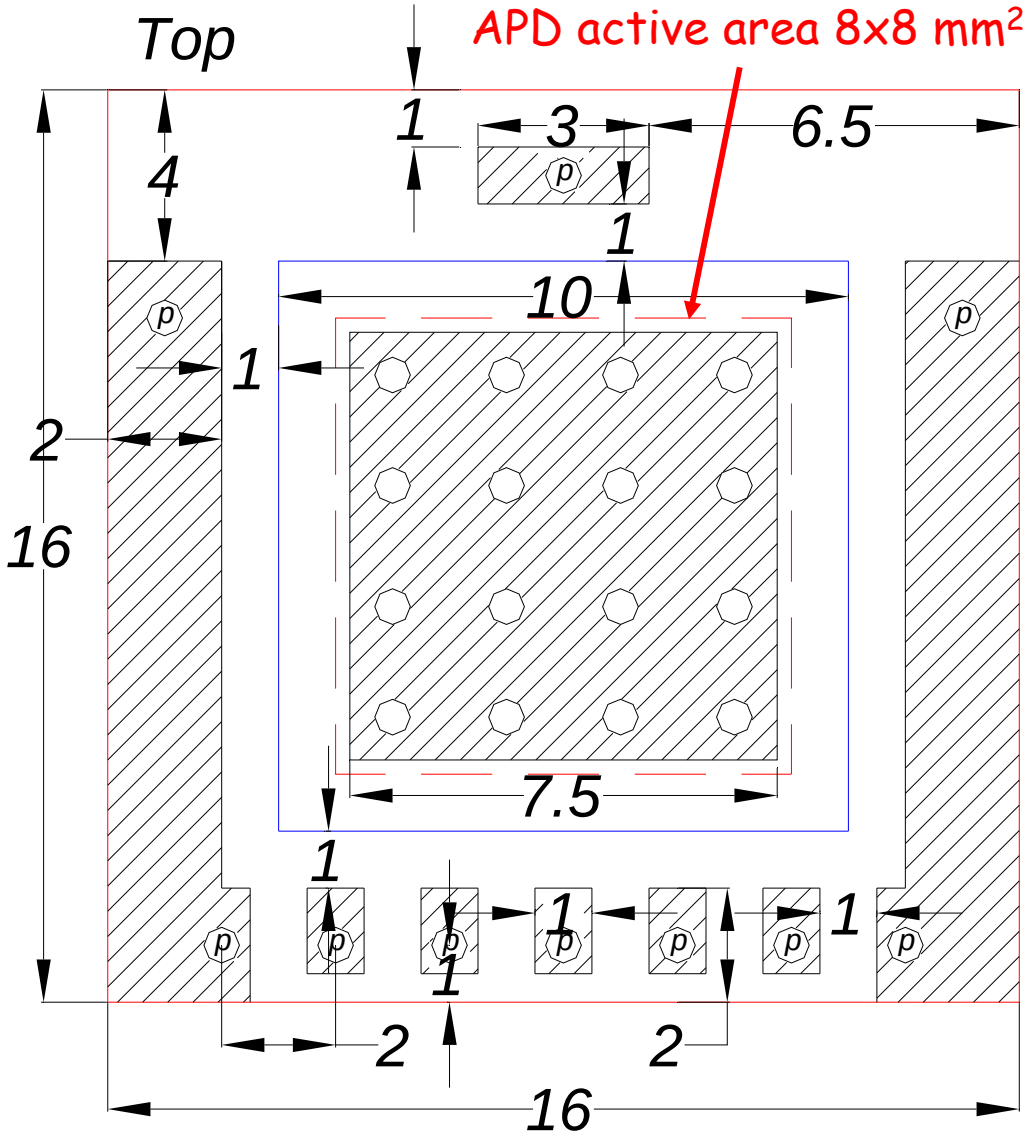
All vias are plated thru, and have pins, soldered on the top side.

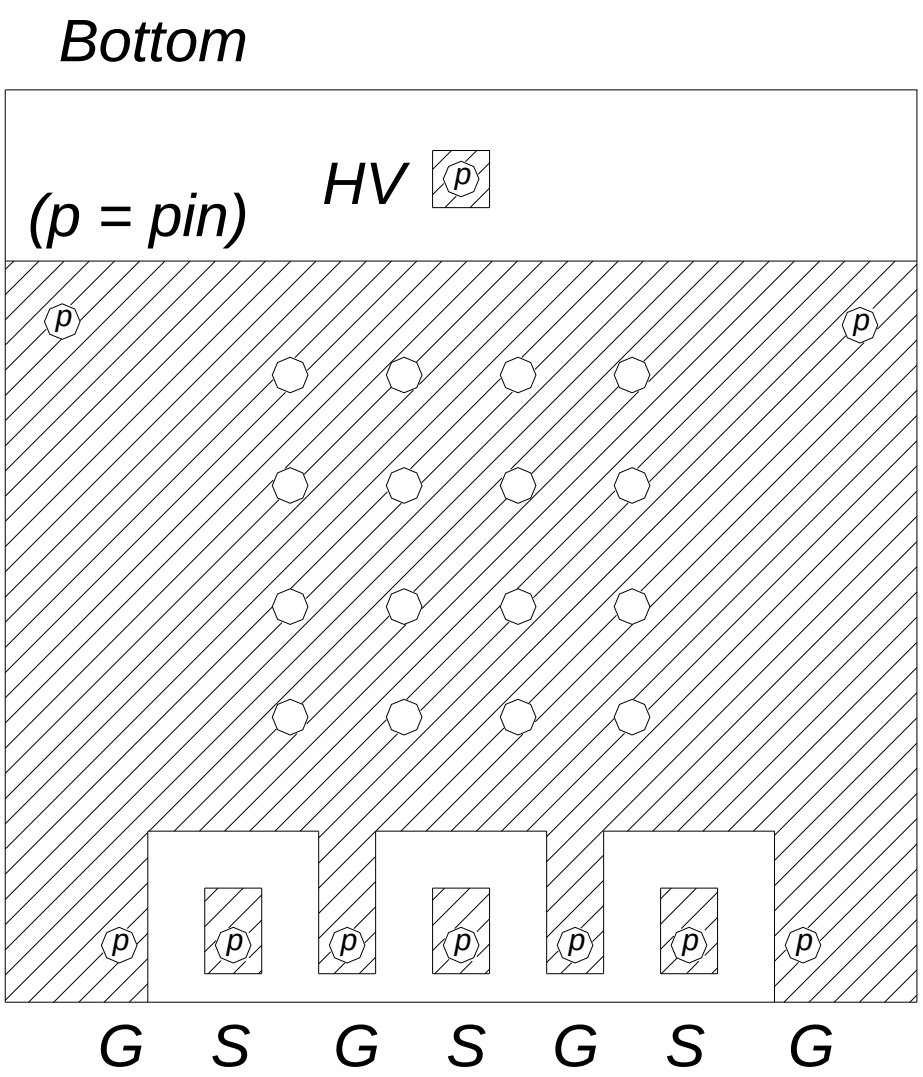
Wire bonds connect the HV and S (signal) solder pads to the APD.

The HV pad, and the HV wire bond, are encased in conformal coating, on both top and bottom of the carrier board.

Tiling

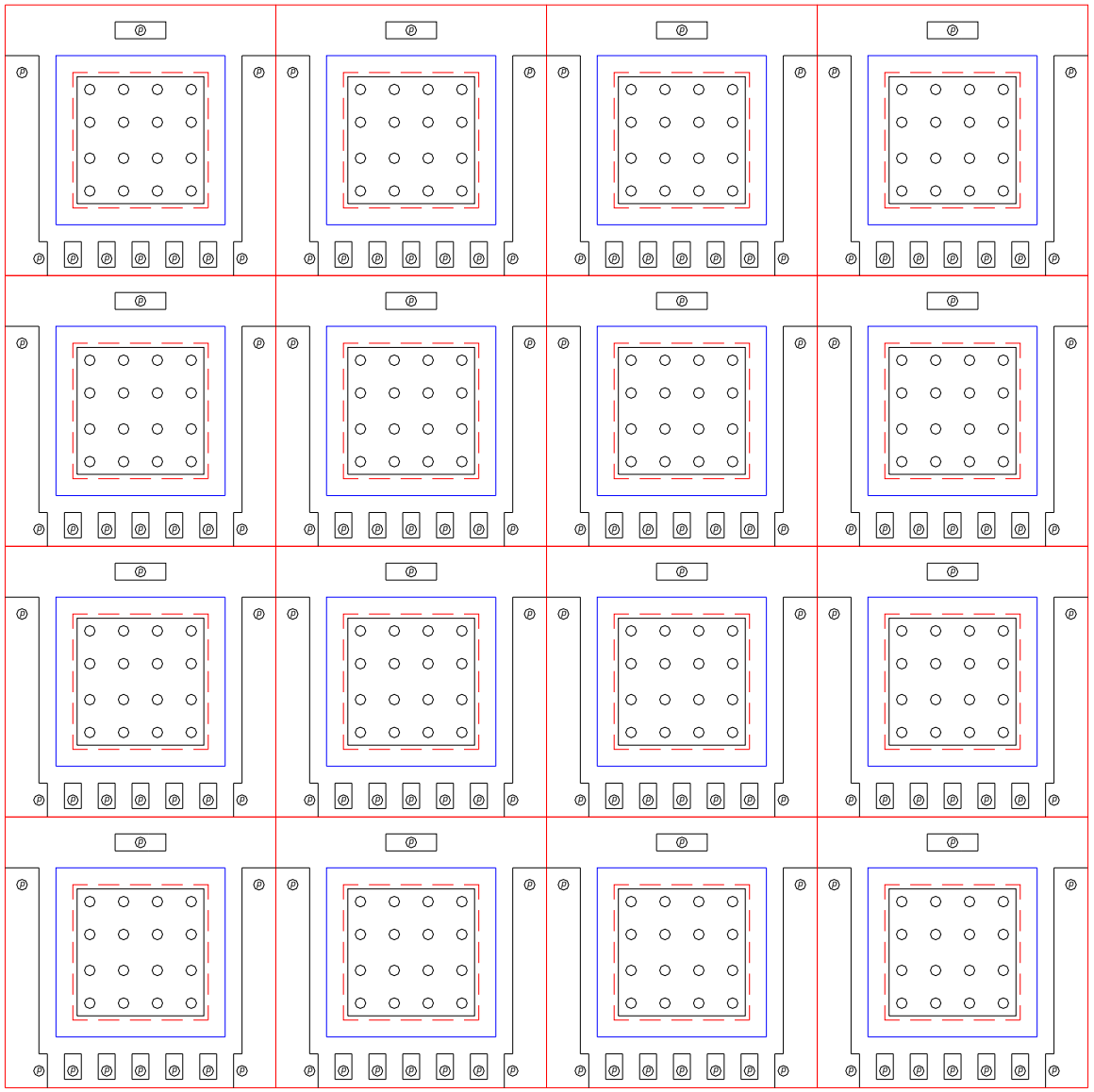
The active area of an APD is 8x8 mm^2.
So, to make a square tiling of such APDs, they could be on a carrier board that is 16x16 mm^2, with 25% active area per layer of tiling, and 4 tiling layers for 100% active area.
The carrier board:



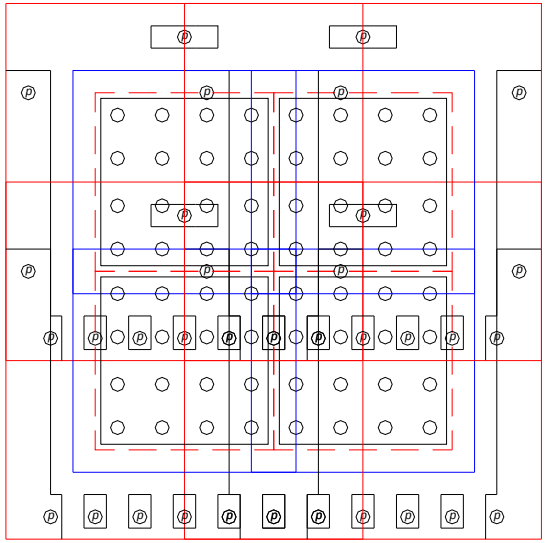


Tiling, II

A single tiling layer, with a 4x4 array of APDs; active area is 25%.



One APD on each of 4 tiling layers, Showing how 100% coverage is thereby obtained



The Penn preamps would be laid in a similar array, with external HV, DC and signal connections along, say the left edge. A multilayer board would facilitate this.