VFE upgrade

Progress report

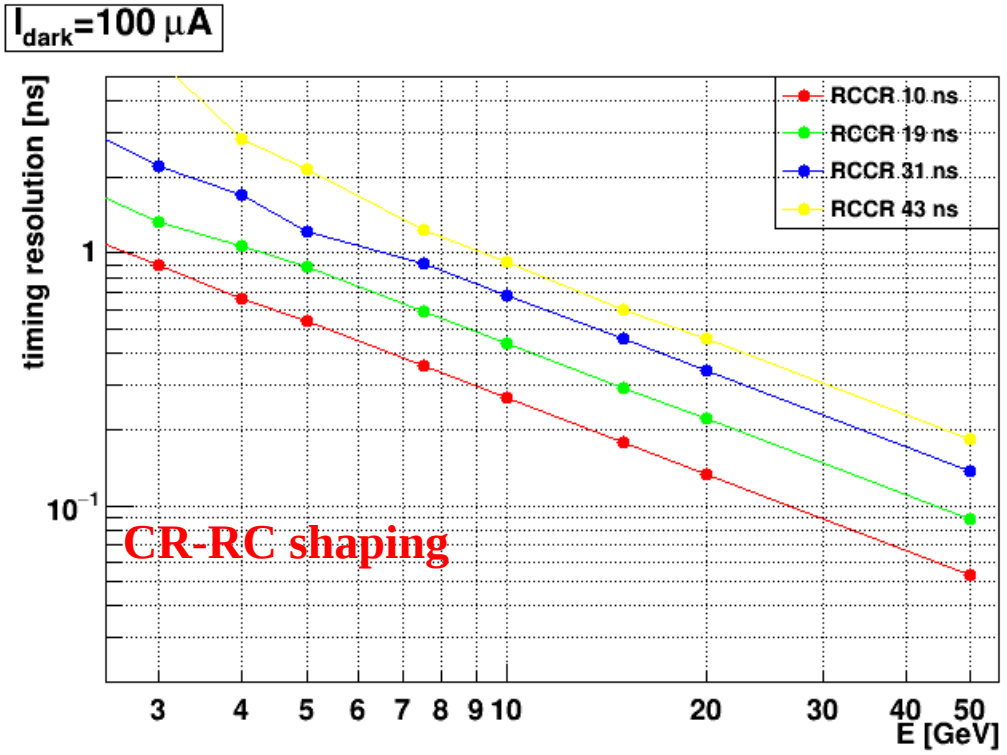
Marc Dejardin
CEA-Saclay Irfu/SPP

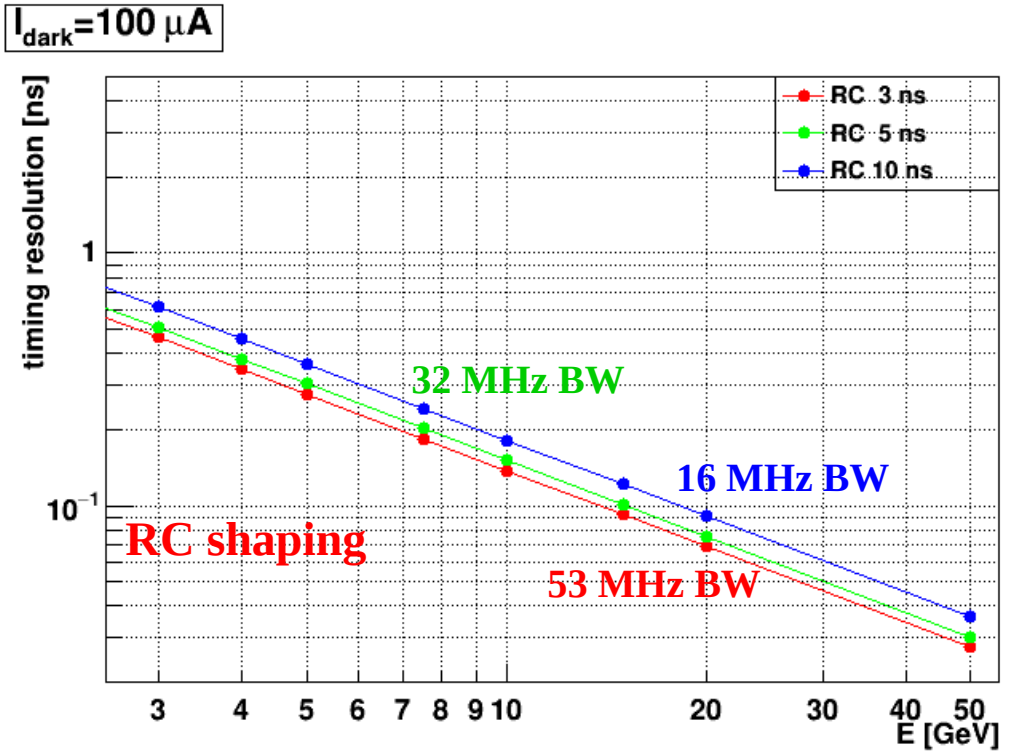
Short term planning

- **Get rock-solid inputs for TDR redaction and further studies/simulations**
  - **Pulse shapes**
    - ► **Scintillation**
    - ► **Spikes**
  - **Noise models**
    - ► **APD leakage current**
  - **ADC**
    - ► **Get VFE performances vs digitization step and sampling rate**
  - **Ultimate timing performances vs E and vs APD aging**
  - **Ultimate energy resolution vs APD aging**
- **How**
  - **Make measurements at TB with fast TIA to get realistic image of physical signals**
  - **Use multi-Gsample/sec ADC to simulate any scenario**

Performance hints

- **Possibility to get good timing information with full signal information**
  - **Worst case scenario (see DN-2015/014)**

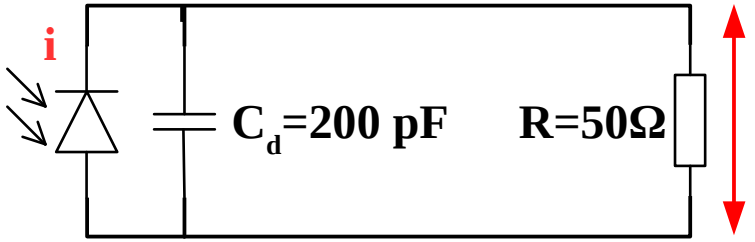




- **Target : 50 MHz BW TIA**
  - **Validate performances at TB**

First try in 2014

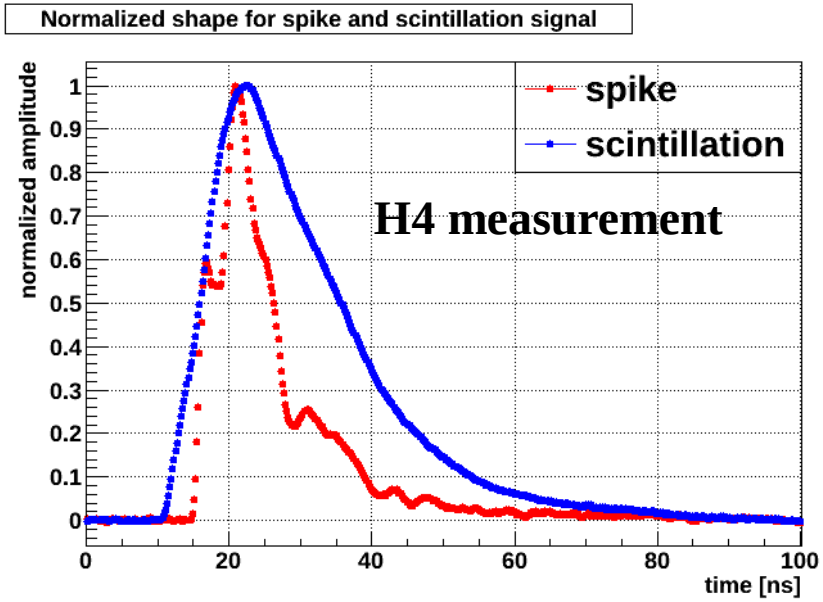
- **Photo-detector has intrinsic capacitance :**

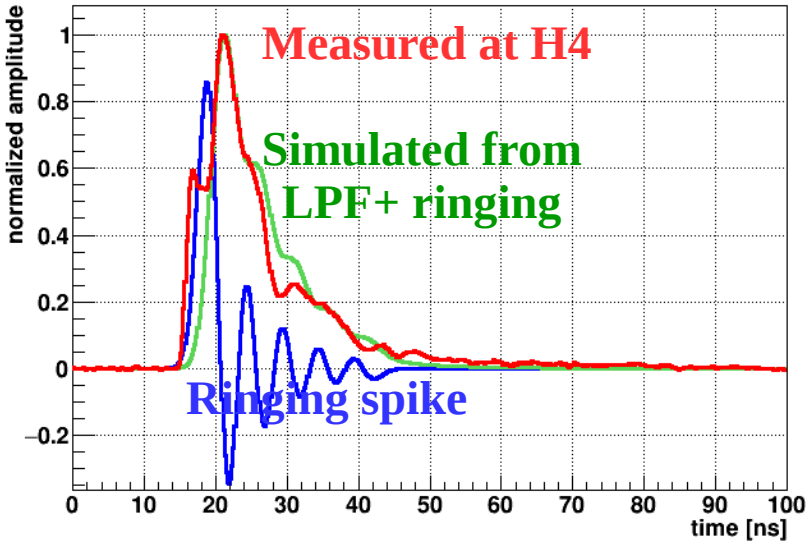


$$s = \frac{R}{1 + RC_d p} i$$

= LPF @ τ_c=10 ns

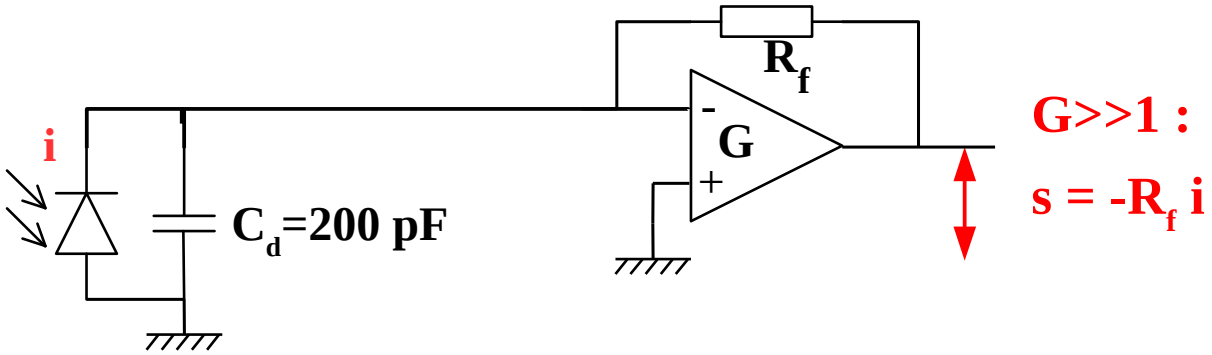
- **Direct connection of APD to digitizer**
  - **Low pass filter**
  - **Kapton connections = RLC circuit**





Ideal TIA

- **Isolate APD from digitizer**
  - **Keep high bandwidth signal**
    - ▶ **APD should see 0 Ω input impedance amplifier → TIA**
    - ▶ **Very high open-loop gain (G) amplifier with feedback resistor (R_f):**
      - **Gain = $-R_f/(1+1/G)$**
      - **Input impedance : R_f/G**



VFE board specifications

- **Requests**
  - **Ready and operational before TB (June ?)**
    - ► **Use of discrete components (No ASIC)**
    - ► **Work on ASIC study in parallel**
  - **50 MHz TIA**
    - ► **Should be able to test ultimate timing performances**
    - ► **Shape measurements**
  - **Low noise (as low as possible)**
    - ► **Should be able to validate APD noise model**
  - **100 MeV- 2TeV dynamics**
  - **2 outputs : Gain 1 and gain 10**
    - ► **Simulate gain switching at LHC**
  - **CMS-ECAL geometry**
    - ► **Should plug on Mother Boards**

Architecture : 50 MHz BW TIA

- **Use discrete components**
  - **Operational amplifiers**
- **50 MHz Bandwidth**
  - **Constraint from APD capacitance**
    - ► **Need > 650 MHz Op-Amp Bandwidth (GBWP)**
  - **Need to “compensate” the gain loop for stability**
    - ► **Capacitor in parallel to gain resistor**

Theory : Expected TIA noise-1

- **Noise sources:**
  - **APD leakage current :**

$$\tilde{i}_{APD} = \sqrt{2 I_d q_e (\epsilon + MF(1-\epsilon))\Delta f} = 5.4\sqrt{I_d}\ nA/\sqrt{Hz}$$

  - **Op-amp input current noise :**

$$\tilde{i}_{OA} \approx 2.5\ pA/\sqrt{Hz}$$

  - **Op-amp input voltage noise :**

$$\tilde{e}_{OA} \approx 1.0\ nV/\sqrt{Hz}$$

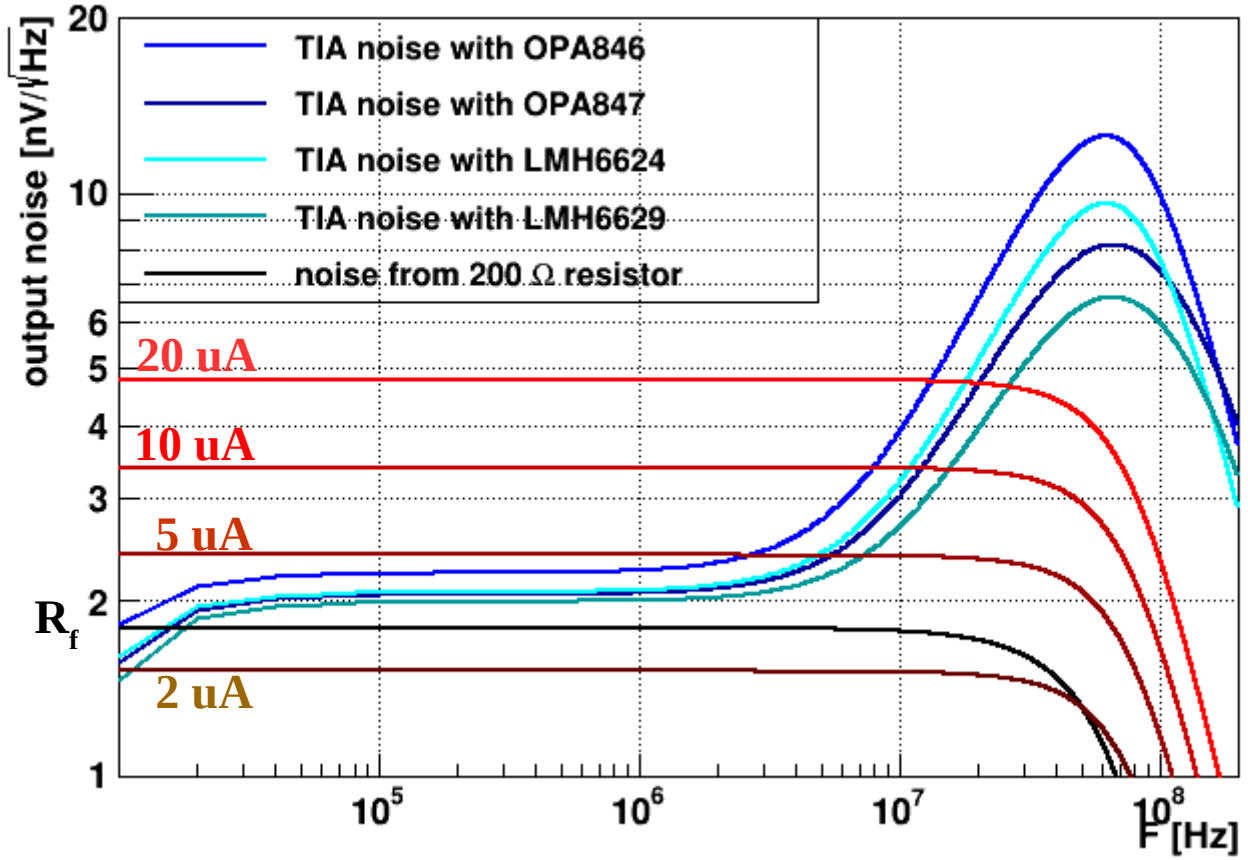
  - **Total output noise :**

$$\tilde{s} = \sqrt{|H|^2 \tilde{i}^2_{leak} + |H|^2 \tilde{i}^2_{OA} + \left| \frac{1 + \frac{R_f}{Z_d}}{1 + \frac{1}{G}(1 + \frac{R_f}{Z_d})} \right| \tilde{e}^2_{OA}}$$

    - ▶ $|R_f/Z_d| \sim R_f C_d 2\pi F$
    - ▶ **Rise at high frequencies !**

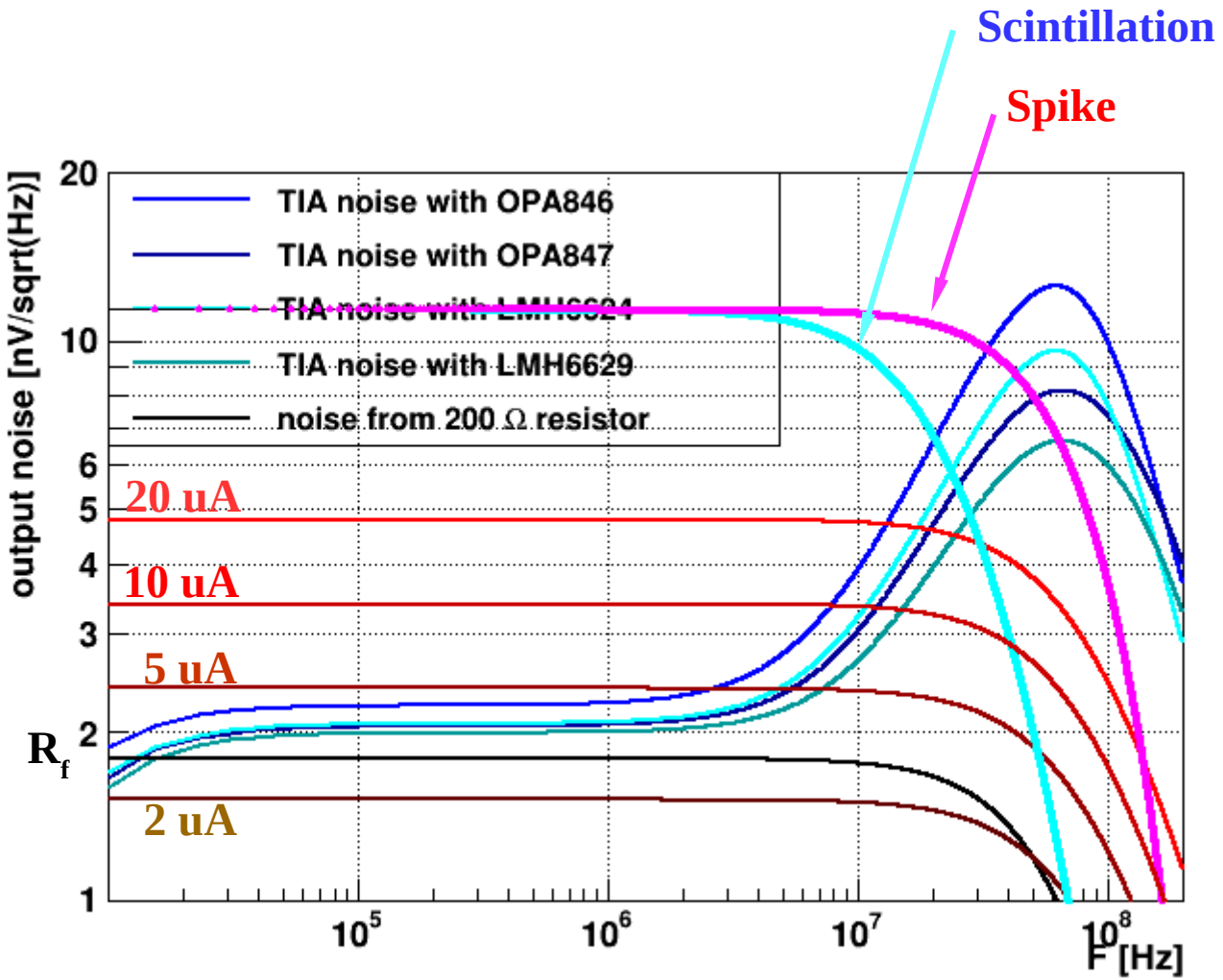
Theory : Expected TIA noise-2

- Compute noise with various amplifiers
- Compare with expected noise from APD leakage current



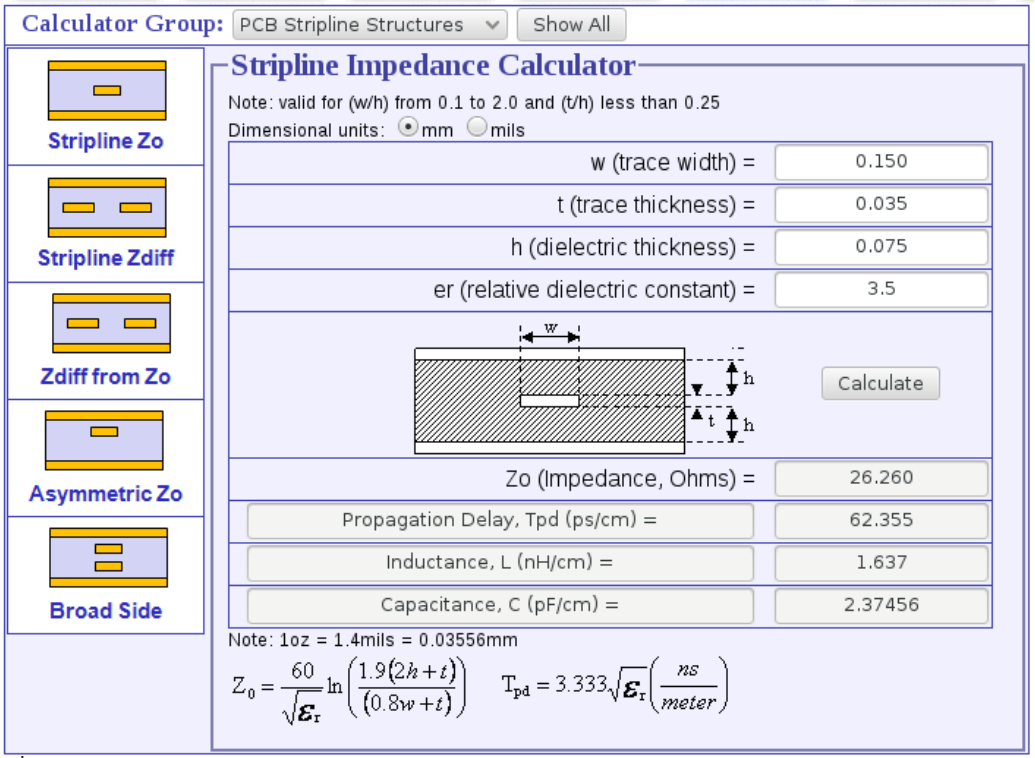
Theory : Expected TIA noise-3

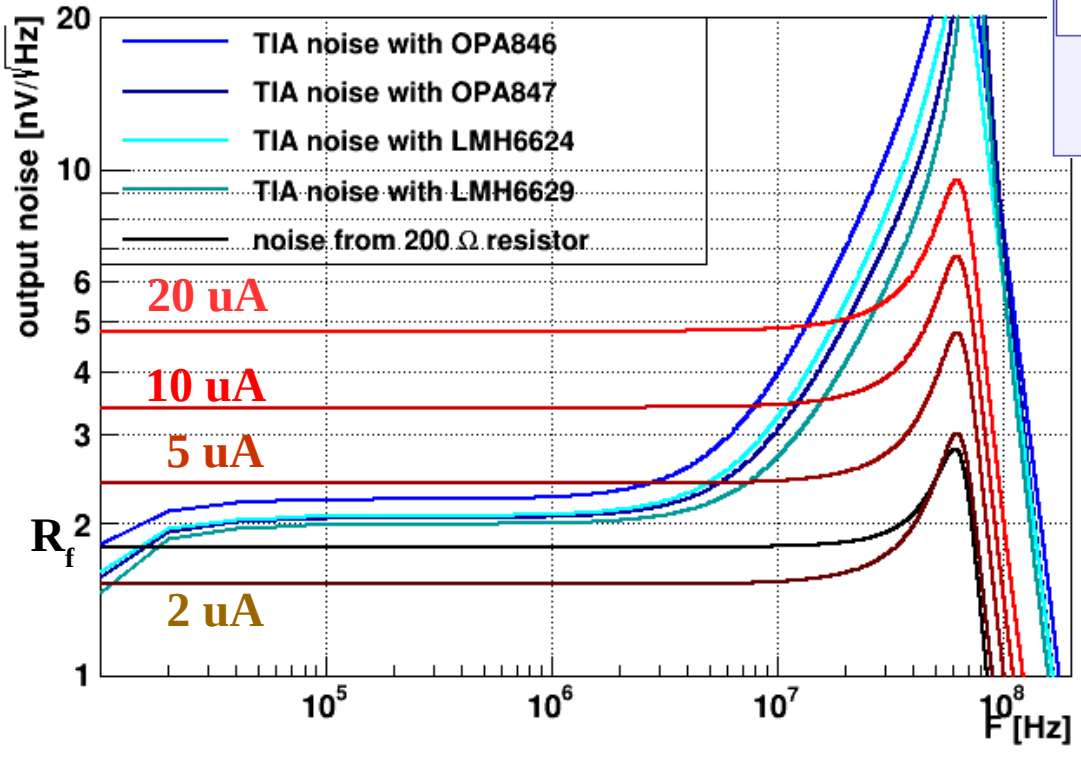
- **Compare with signals**

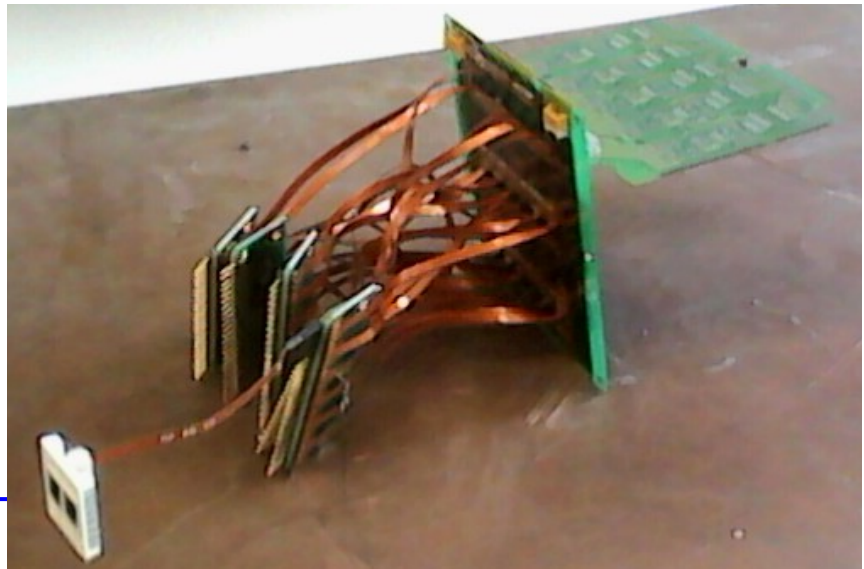


Fit with ECAL geometry : Effect of APD kaptons

- **Add inductance between APD and TIA**
  - **Estimated to 2.4pF/cm and 1.6 nH/cm**
    - ► **Huge distortion of frequency response**
    - ► **Noise enhancement**

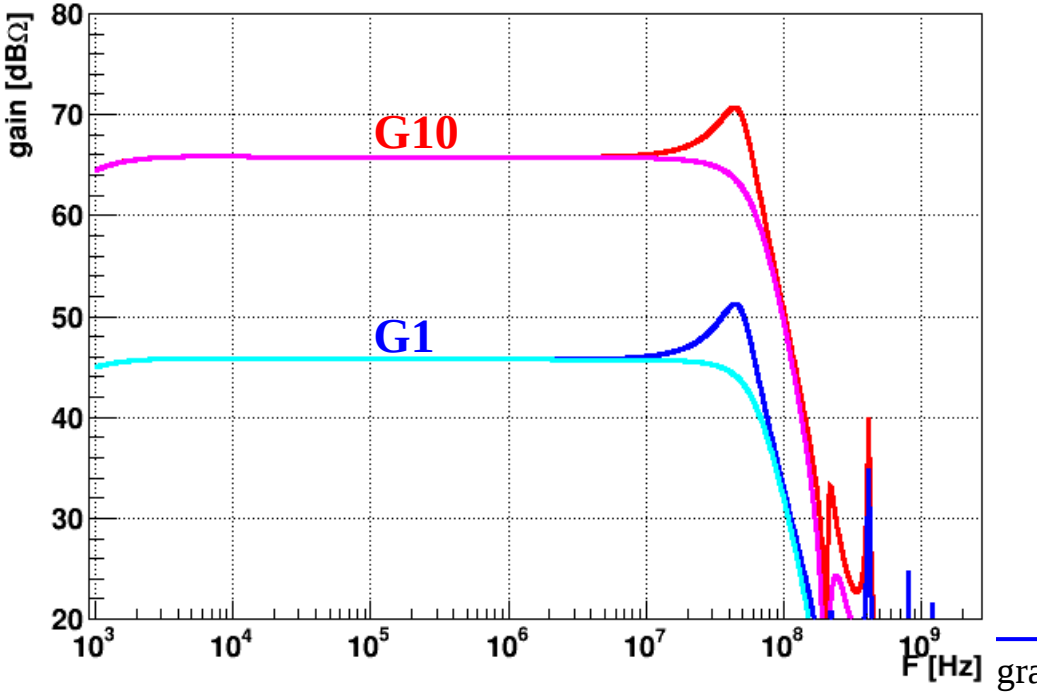


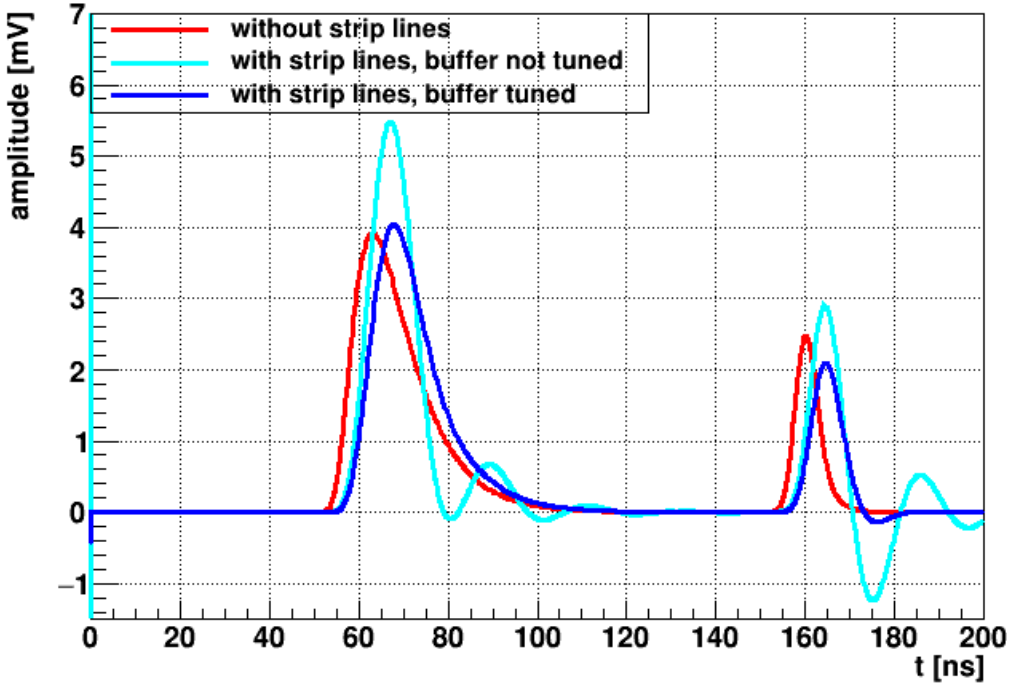




Towards VFE board

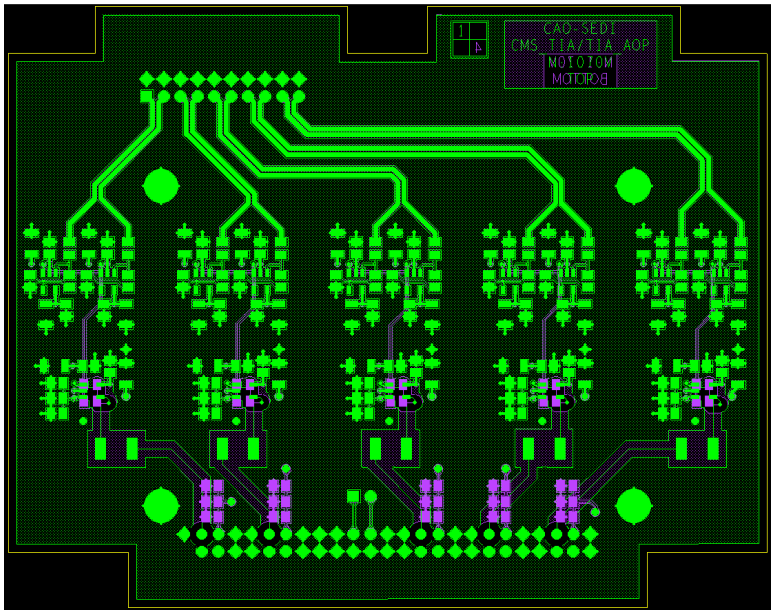
- **Optimize design**
  - **Low Noise**
  - **Kapton effect:**
    - ▶ $L_{kapton}C_{APD}$ → 63 MHz resonator -> above 50 MHz BW → OK
  - **Kapton mitigation : add serial (damping) resistor on APD line**
    - ▶ Keep 50 MHz bandwidth
    - ▶ Restore pulse integrity



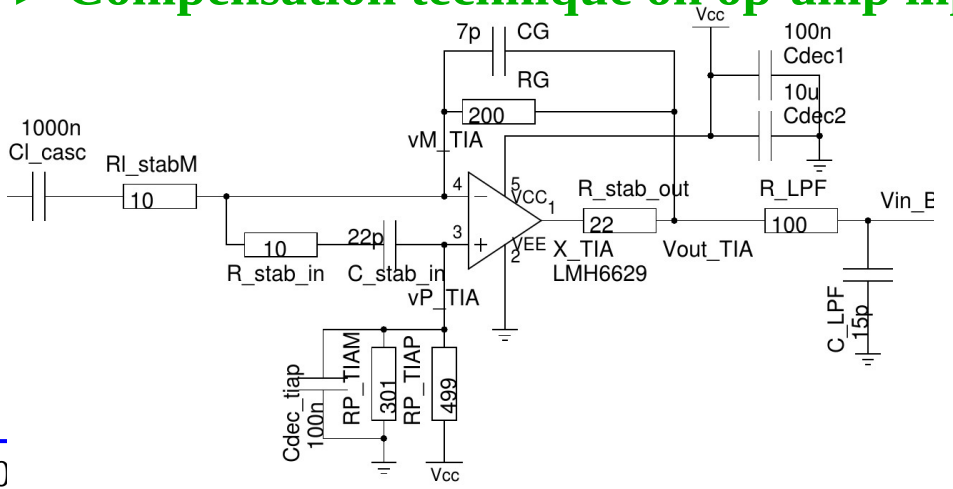


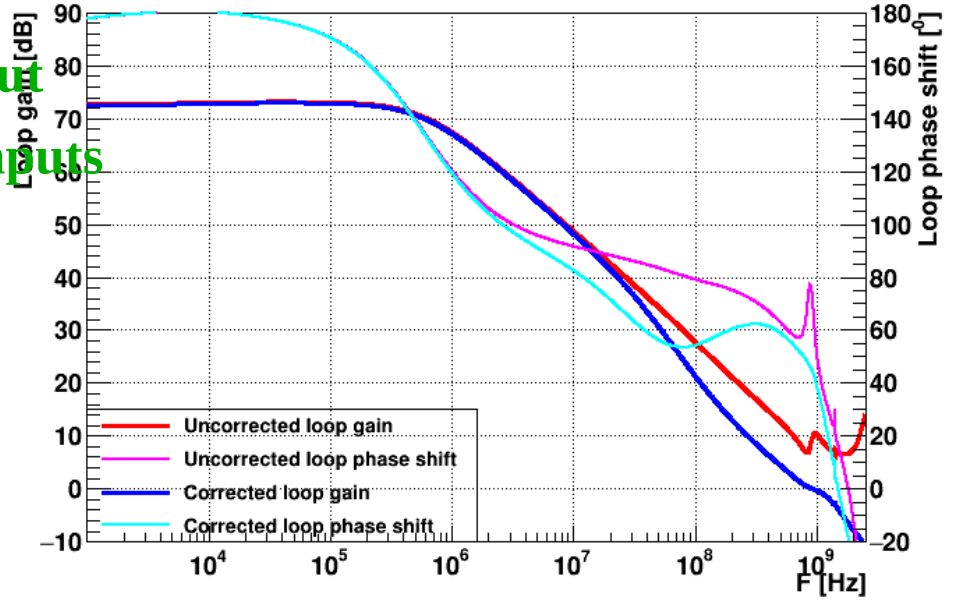
Real life

- **Build a VFE board with Op-amp TIA**
  - **500 MHz Oscillator :(**
  - **LMH6629 very sensitive to parasitic inductances**
    - ► **0.55 nH/mm + 1.2 nH/via on PCB**
    - ► **Not taken into account**



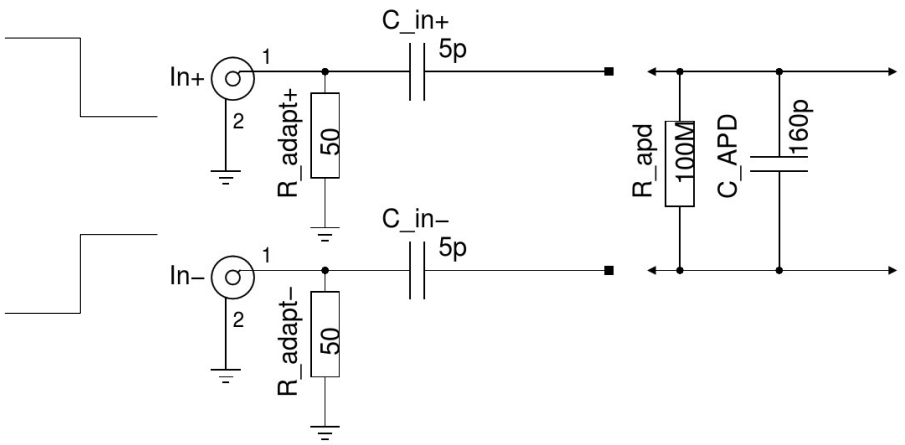
- **Modify PCB in situ**
  - **Restore phase margin**
    - ► **Add damping resistor on op-amp output**
    - ► **Compensation technique on op-amp inputs**





Performances

- **Noise measurements**
  - **Connect TIA output to Digital scope**
    - ► **Measure RMS**
    - ► **Measure noise density spectrum using FFT in Math tools**
- **Signal Measurements**
  - **Inject current pulses through capacitors [i(t)=C dV/dt]**
    - ► **Spike simulation using very fast edged signals (0.9 ns)**



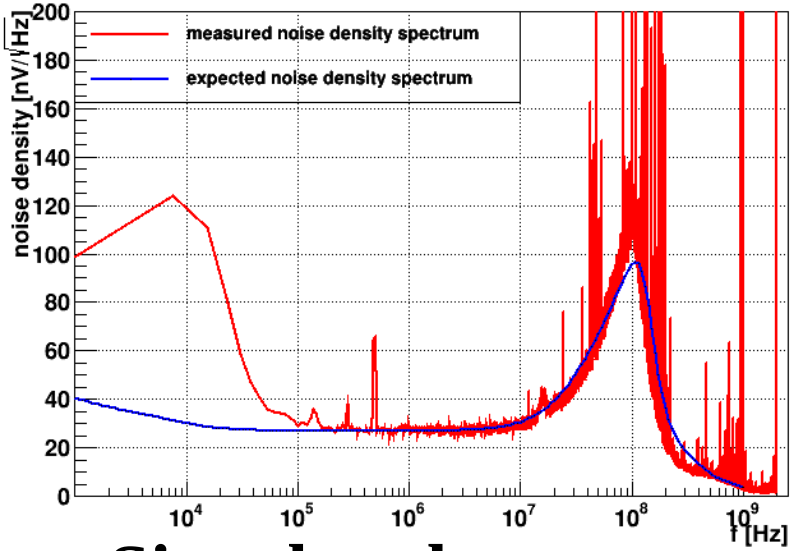
Spike injector

Noise generator

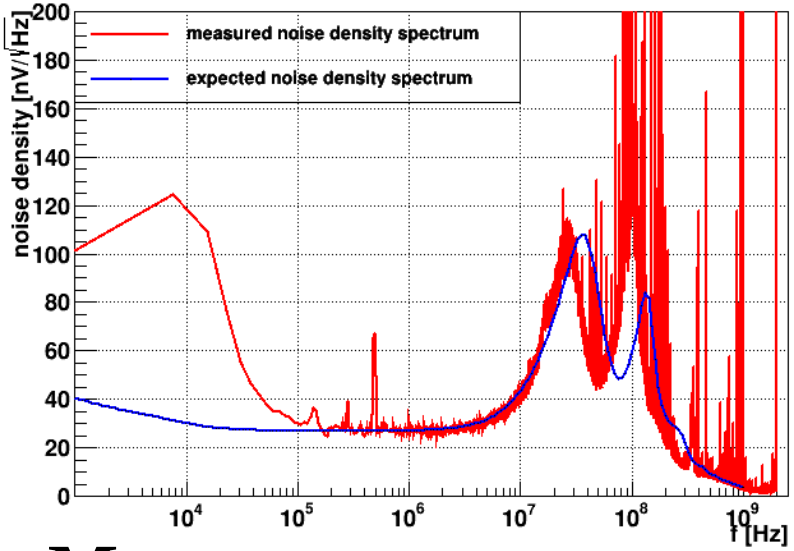
First iteration results

- **Noise density spectra: Spice vs Measurements**

F2fft-g10_noise-0pF_dB — No APD connected

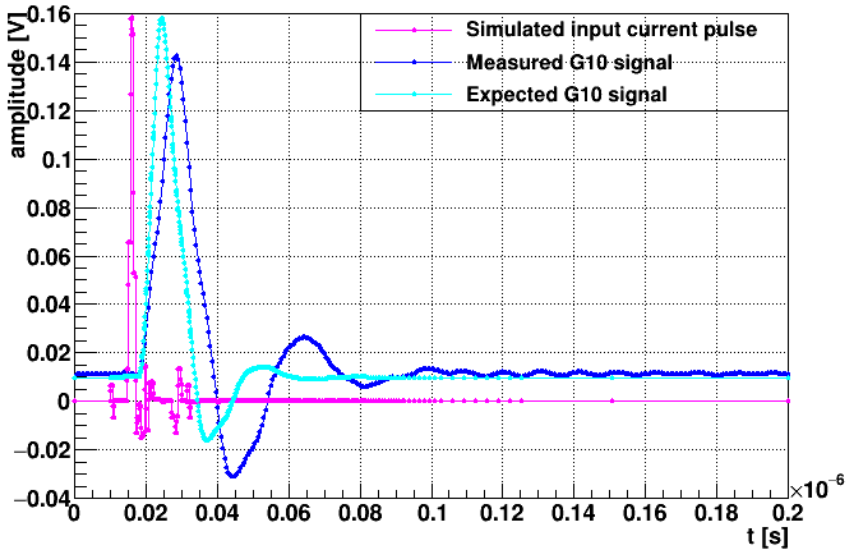


F2fft-g10_noise-164pF_dB — Fake APD connected

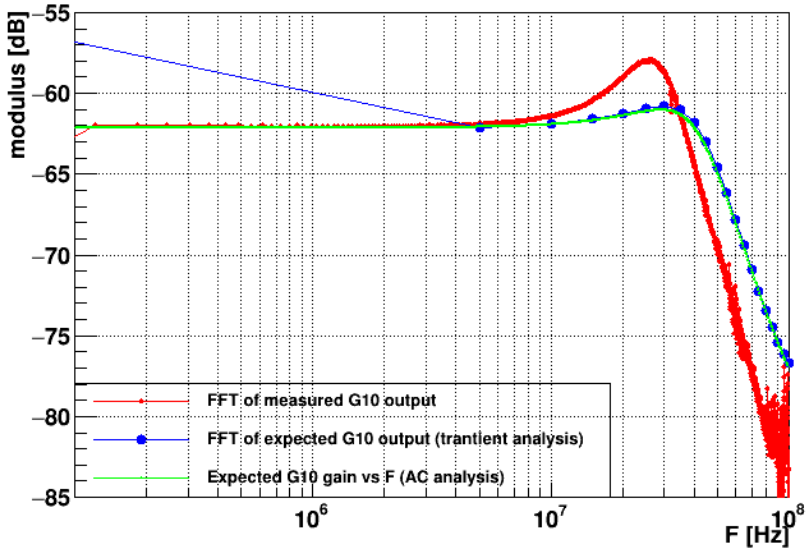


- **Signal and spectrum: Spice vs Measurements**

Simulation with 1.6nH/cm and 2.4pF/cm



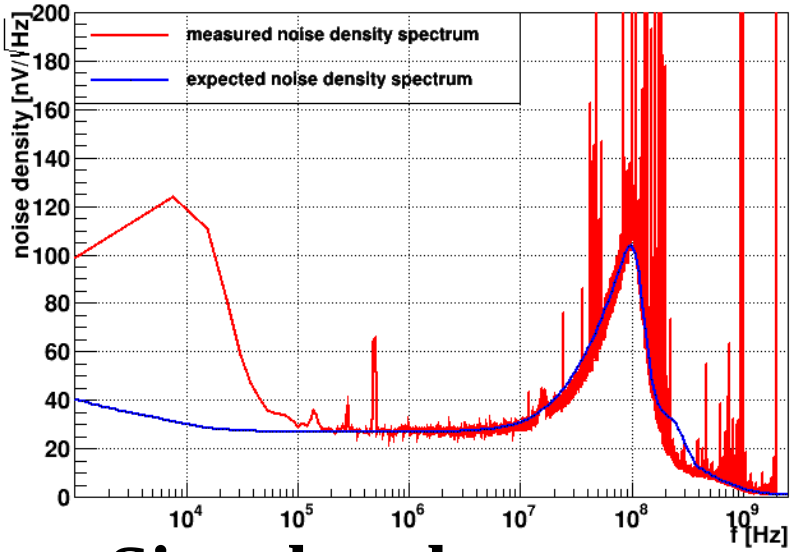
G10 output spectrum (1.6nH/cm, 2.4pF/cm)



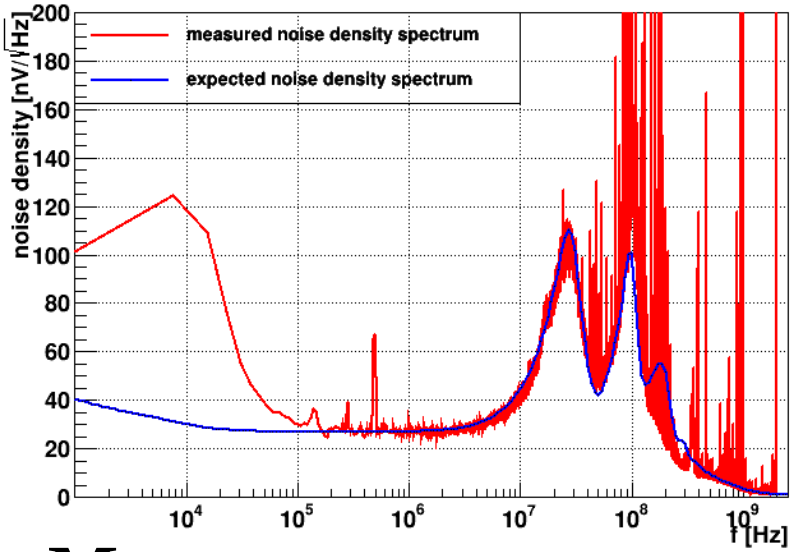
Tune kapton characteristics

- **Noise density spectra: Spice vs Measurements**

F2fft-g10_noise-0pF_dB — No APD connected

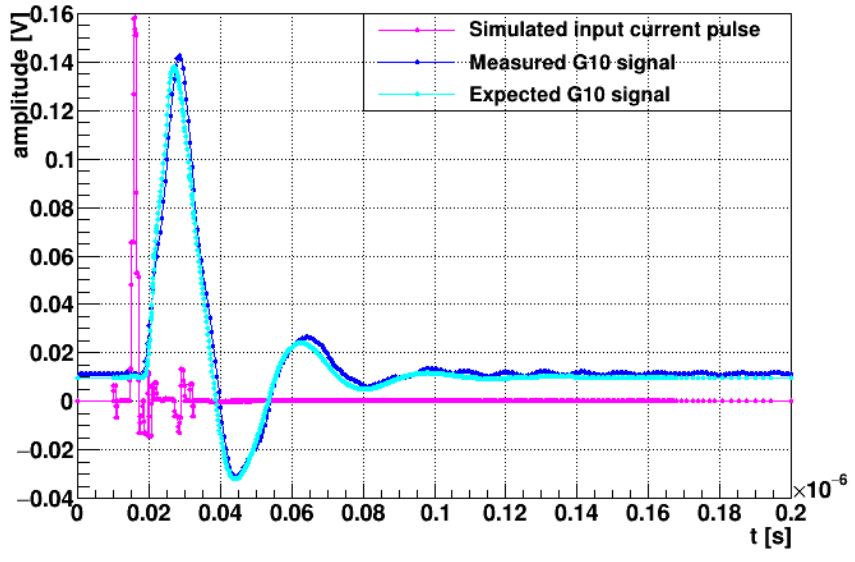


F2fft-g10_noise-164pF_dB — Fake APD connected

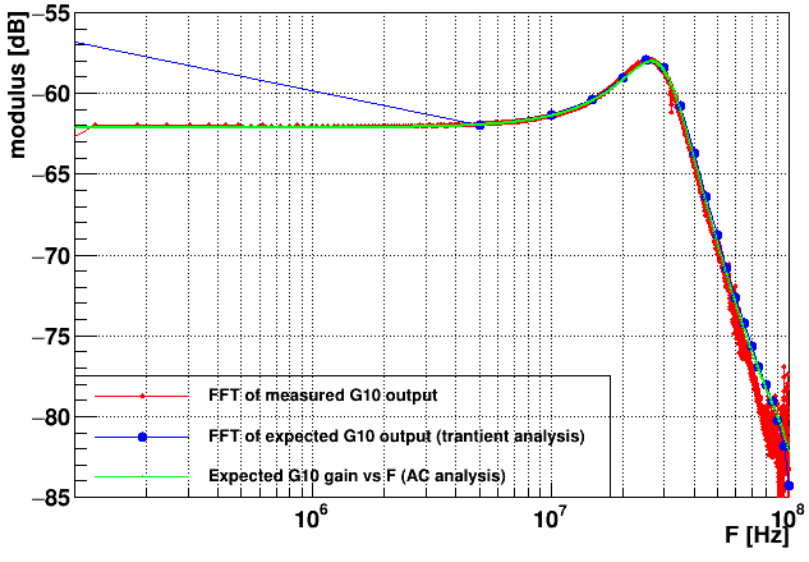


- **Signal and spectrum: Spice vs Measurements**

Simulation with 3.75nH and 2.5pF/cm

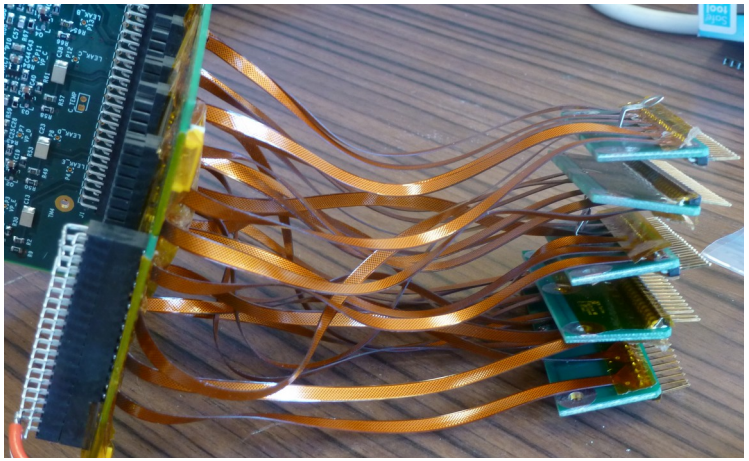


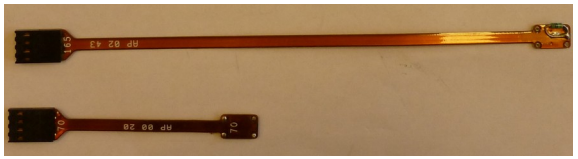
G10 output spectrum (3.75nH/cm, 2.5pF/cm)



Kapton parameters

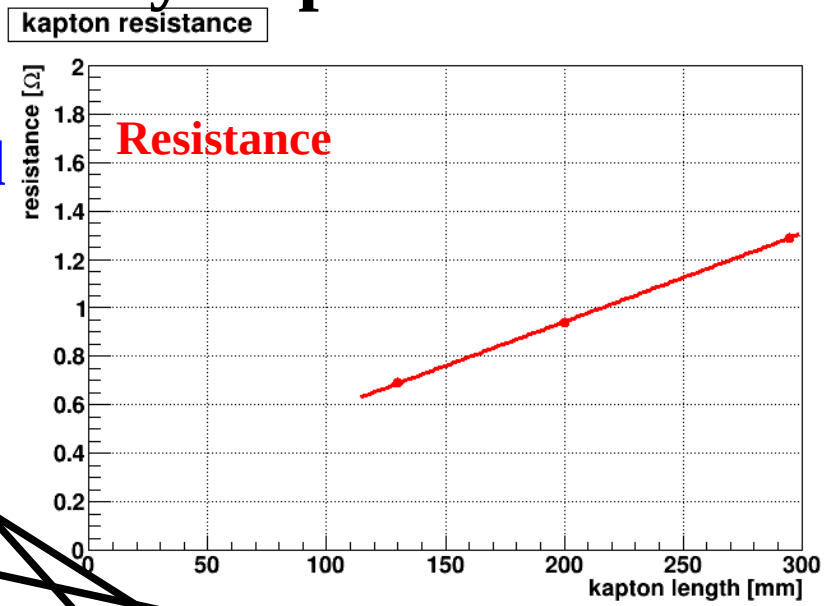
- Good spice-measurement agreement with
  - 3.75 nH/cm instead of 1.6nH/cm
  - 2.5 pF/cm instead 2.4pF/cm
- Make measurements on kaptons
  - Back to lab
    - ► Use HP4194 from past century
    - ► I/O is only screen or printer

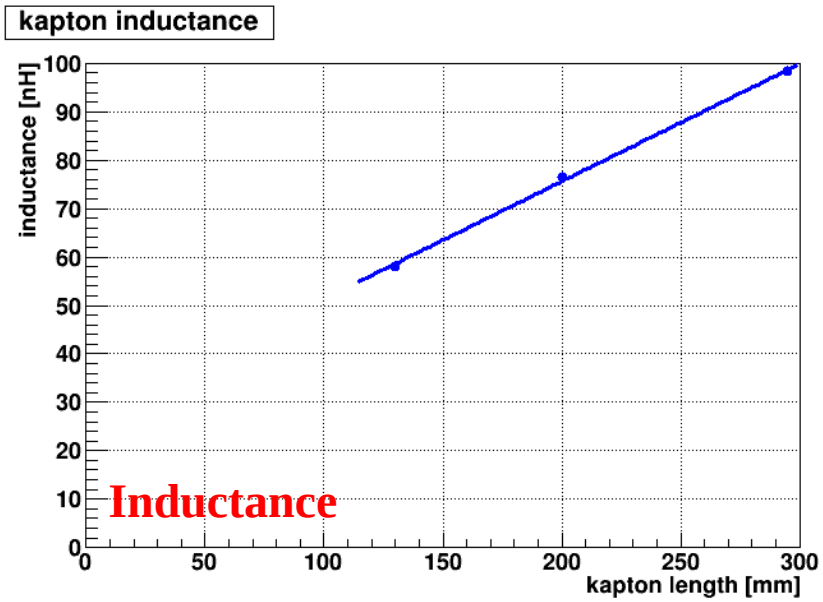


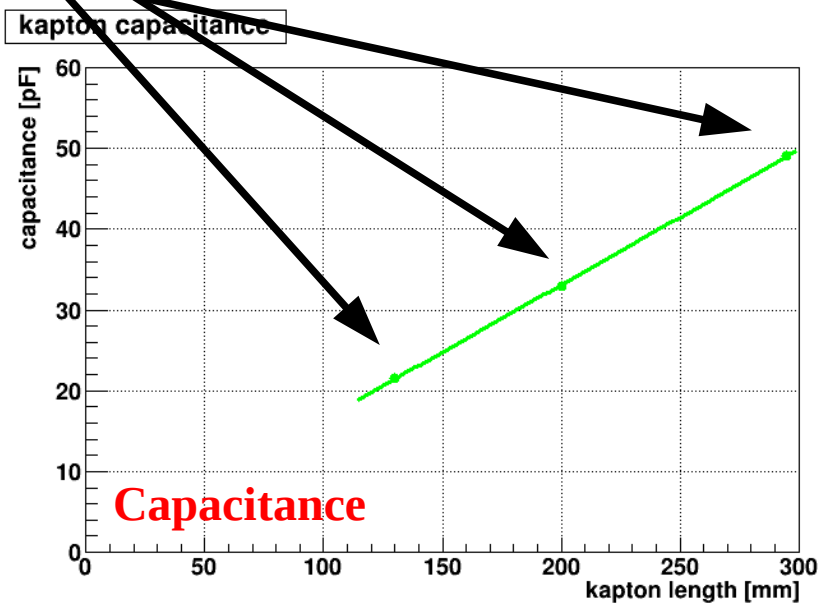


Kapton measurements-1

- **Automatic measurement of frequency response**
  - **From 10 kHz to 100 MHz**
  - **Compute equivalent R-L-C model**
- **Measurements**
  - **Mother-board alone : 13cm**
  - **+ Module 1 kapton : 70 mm**
  - **+ Module 4 kapton : 165 mm**





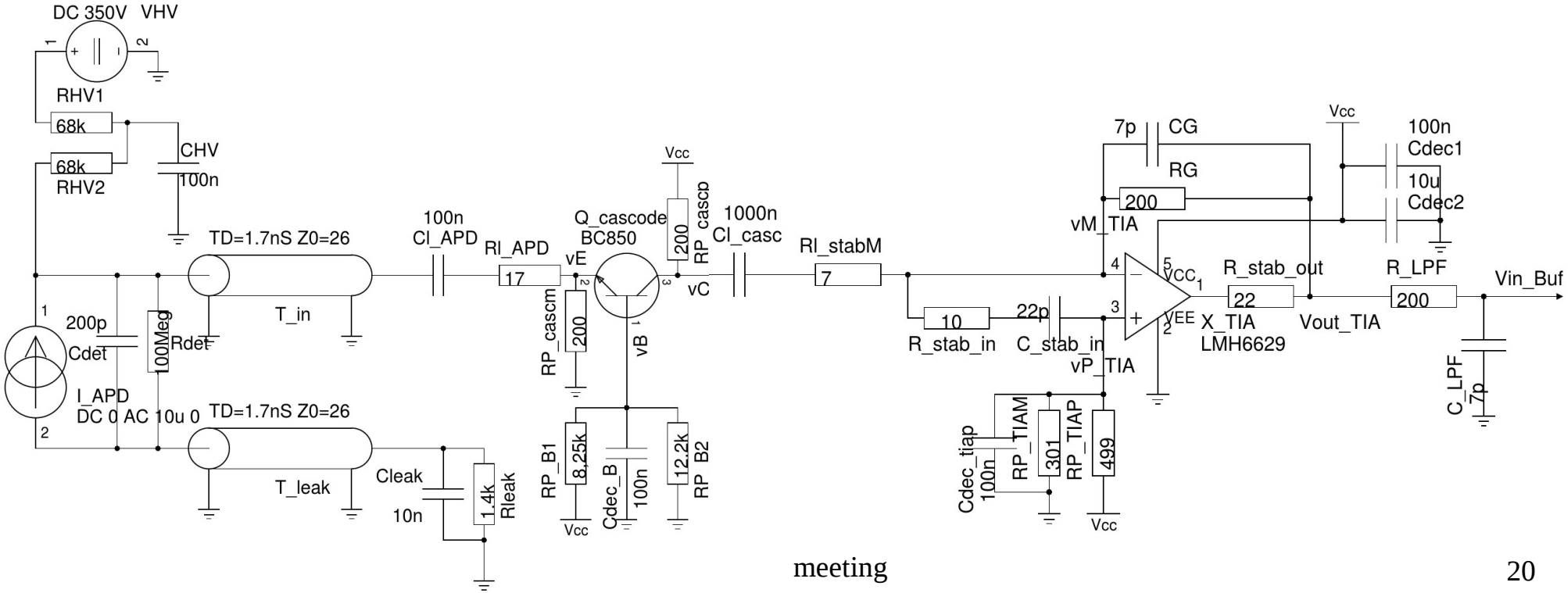


Kapton measurements-2

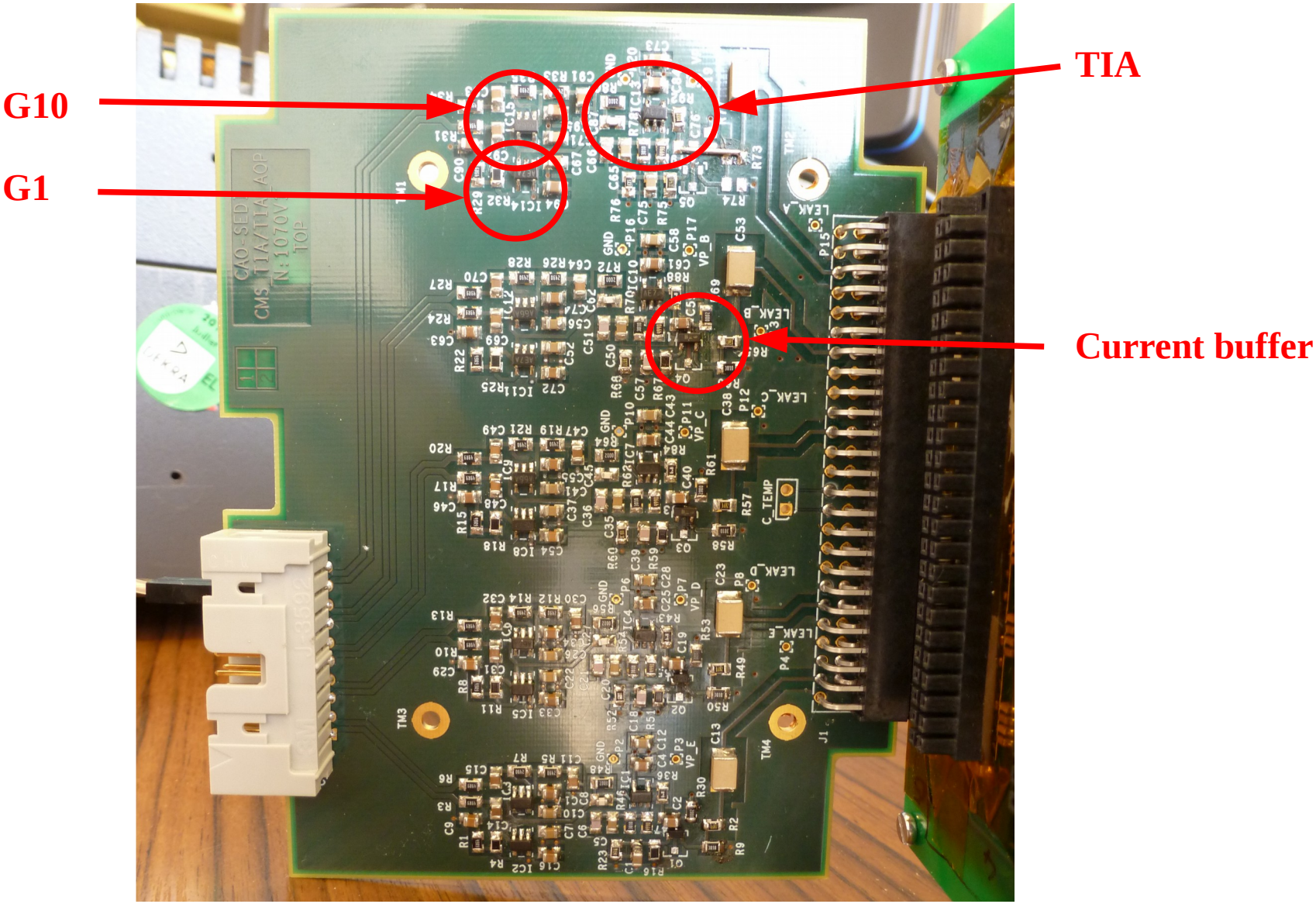
- Curves “R-L-C vs d” don't go through 0
  - Mother boards and capsules kaptons are different
- Mother board kaptons (d = 130 mm)
  - R_{MB} = 53 mΩ/cm
  - L_{MB} = 4.5 nH/cm
  - C_{MB} = 2.4 pF/cm
- APD capsule kaptons (d from 70 to 165 mm)
  - R_APD = 35 mΩ/cm
  - L_APD = 2.4 nH/cm
  - C_APD = 1.7 pF/cm
- Possible impedance mismatch at capsule connection
- Dramatic consequence:
  - Shift resonance frequency below 40 MHz
    - ► Inside signal frequency domain !

Second iteration

- **New PCB with reduced parasitics**
  - **Optimized for low kapton parameters (not measured ones)**
- **Modified input stage**
  - **Possibility to insert a current buffer between APD and TIA**
- **Modified TIA stage**
  - **Implement compensation for phase margin recovery**

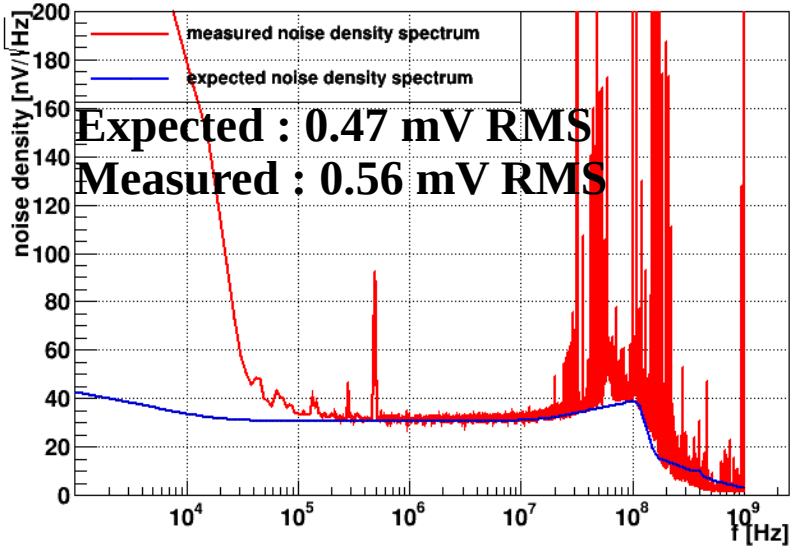


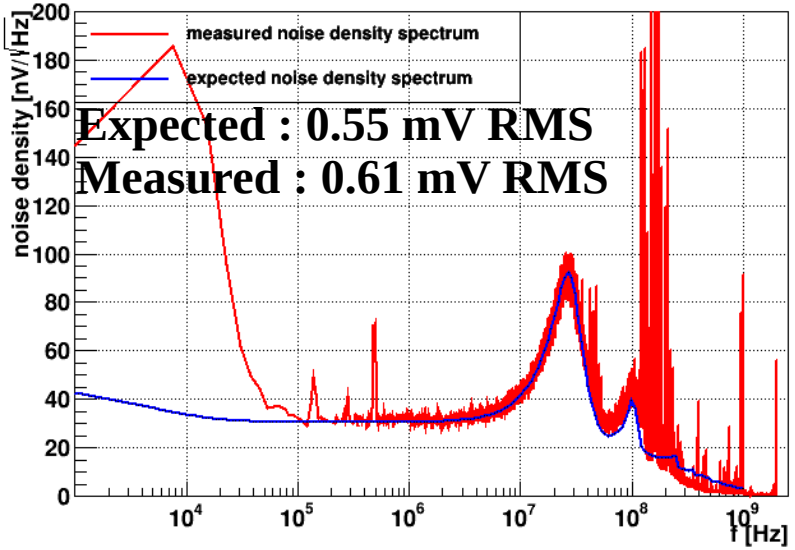
New PCB



Performances without current buffer

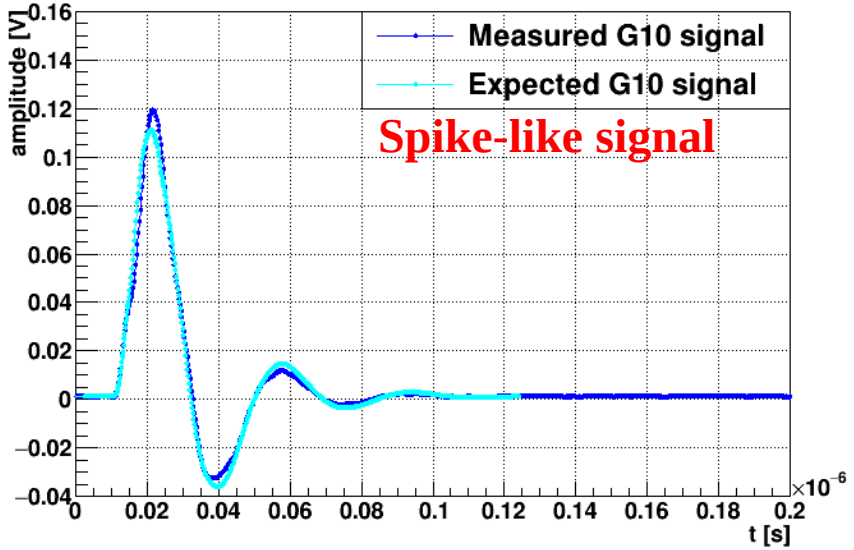
- Use measured kapton parameters
- Noise



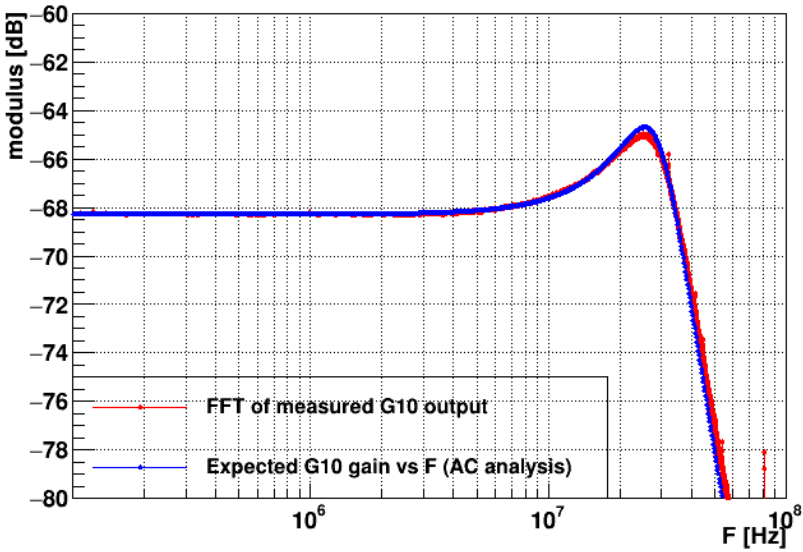


- Signal

Simulation with measured kapton parameters



G10 output spectrum (measured kapton parameters)

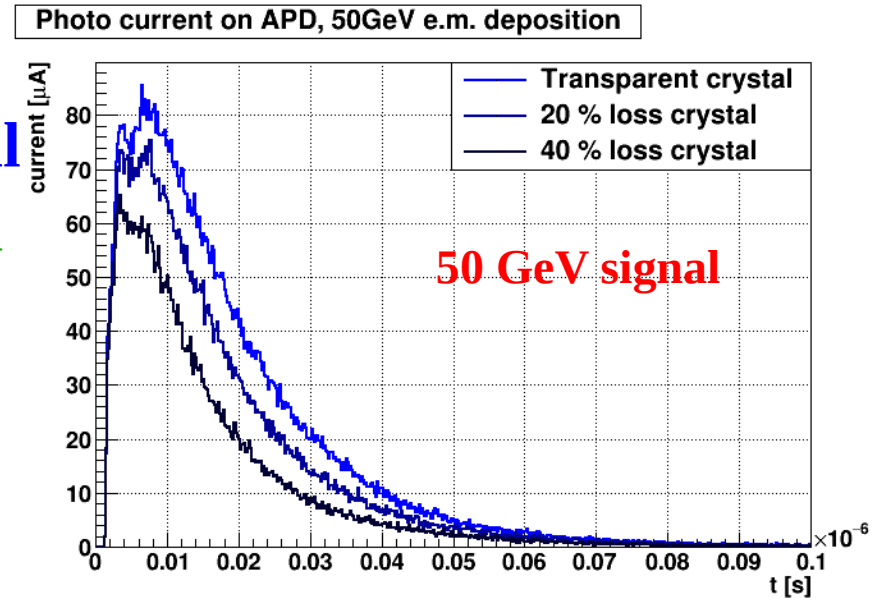


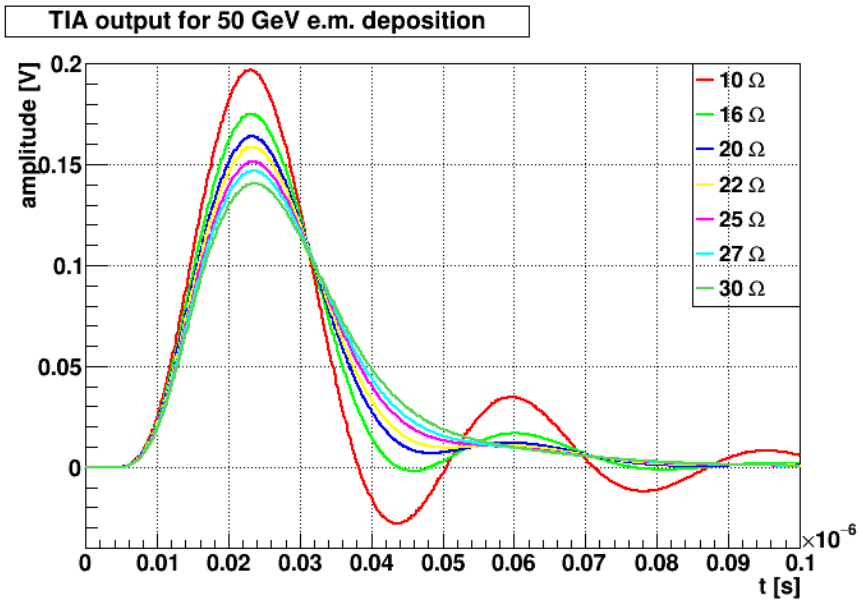
Performances with current buffer

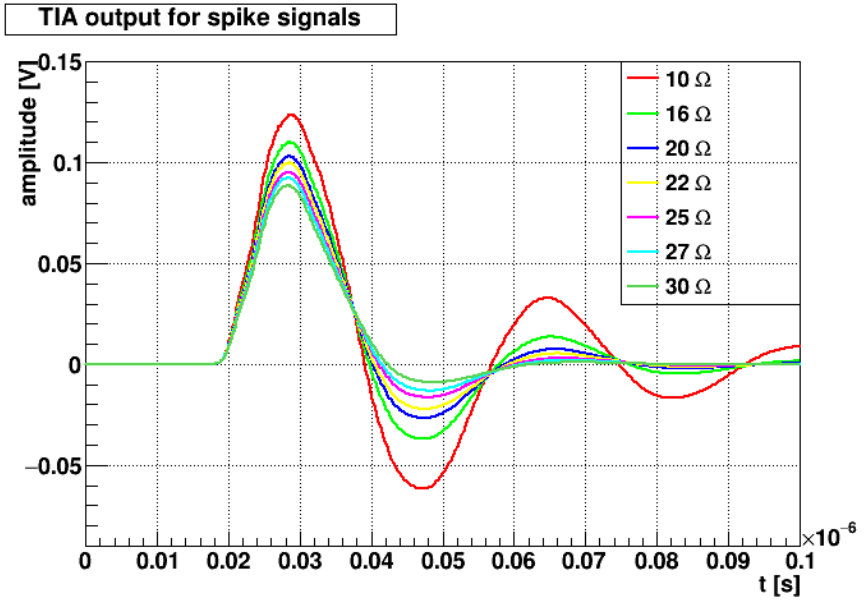
- **Goal**
  - **Isolate TIA from APD connection**
    - ► **Gain stability**
    - ► **Less noise (hopefully)**
- **Problems**
  - **Design optimization with spice but:**
    - ► **Transistor spice models not reliable**
  - **Non predictive study**
- **Work in progress**
  - **Stay tuned**

Mitigating ringing

- **Tune APD damping resistor**
  - **Look at expected scintillation signal**
    - ► **Home made photon tracking program**
    - ► **Generate spice input files for 50 GeV photon**
  - **Simulate TIA response**

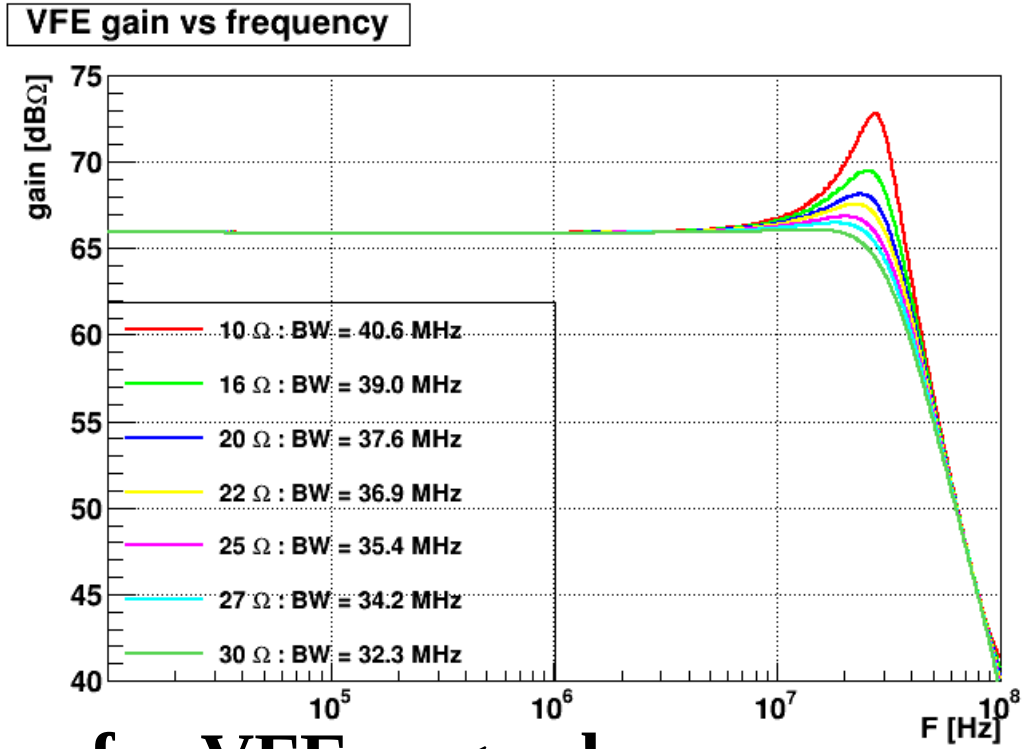






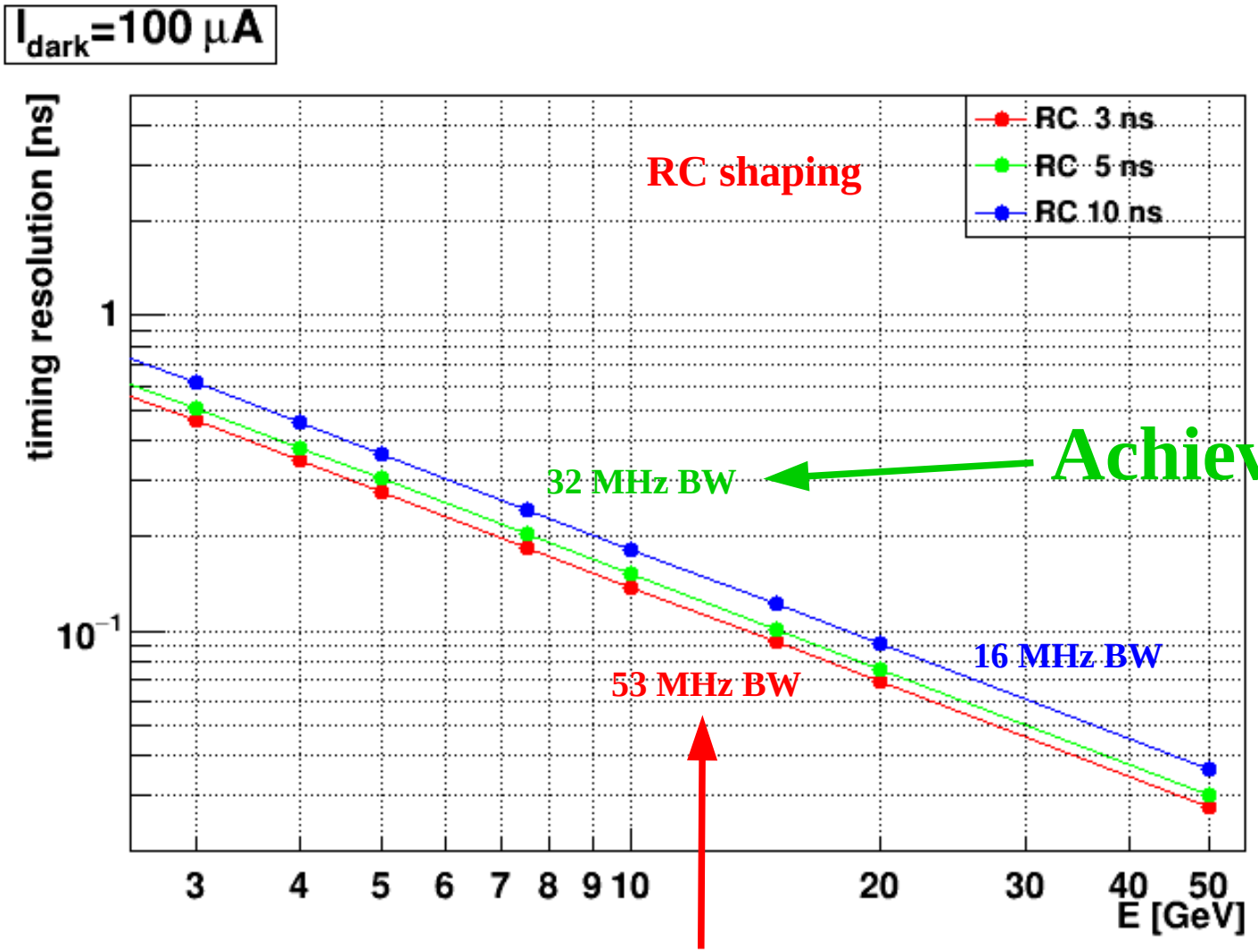
TIA bandwidth vs mitigation

- **Adding serial resistor for kapton mitigation**
  - **Reduces TIA bandwidth**



- **Consequences for VFE upgrades :**
  - **50 MHz bandwidth not achievable !**
  - **Upper most achievable electronics bandwidth : 40 MHz**
  - **Most probable electronics bandwidth 35 MHz**

Consequences



Achievable

Our dream

Next steps

- Check “current buffer” architecture performances
- Connect APD and send light
  - 500 ps laser to simulate spike signal
- Equip 5 VFE boards
  - PCB in hands
  - 2/3 weeks work
- Put in TB
  - Measure scintillation/spike shapes
    - ► Check timing performances
  - Measure noise structure
    - ► Different APD leakage current
- Implement models/shapes in simulation program
- Check performances with Physics (CMSSW)

Conclusions-1

- **VFE upgrade performances limited by existing connections to crystals**
  - **Have to deal with 75-100 nH inductances**
    - ► **System bandwidth limited to ~35 MHz**

- **Preliminary step for:**
  - **Feasibility study of a TIA-asic with TSMC 130nm technology**
    - ► **Study well advanced in Saclay**
    - ► **All simulations OK so far**
    - ► **Signature of CERN-TSMC NDA to go further**
  - **More details at ACES-2016**

Conclusions-2

- **Rock solid inputs mandatory for TDR redaction.**
  - **APD+kaptons+motherboard characterization**
  - **Shape measurement for scintillation and spikes**
  - **Noise models validation**
- **Test-beam measurements with TIA can allow to do this**
  - **~~50~~ 35 MHz BW, reasonable noise level (200 MeV)**
  - **Multi-Gs/sec acquisition to simulate all scenarios**
  - **Fast timing setup to get the timing performances**
- **TIA with Op-Amps designed**
  - **Ready to go to TB with 3 weeks notice**
    - ► **Fine tuning in progress**