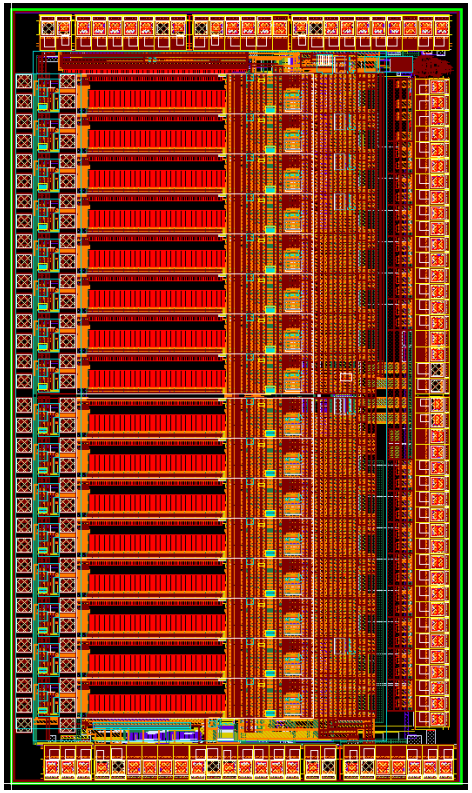

VERY FIRST RESULTS WITH THE LAST VERSION OF SAMPIC

D. Breton[2], E. Delagnes[1], H. Grabas[1,3], O. Lemaire[2], J. Maalmi[2], P. Rusquart[2], P. Vallerand[2]

[1] CEA/IRFU Saclay (France)
[2] CNRS/IN2P3/LAL Orsay (France)
[3] Now with SCICPP Santa Cruz (USA)

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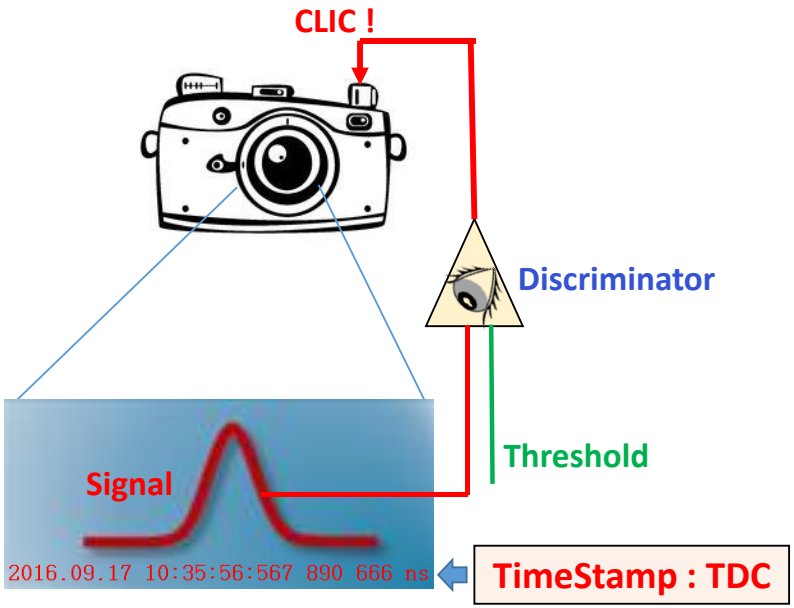
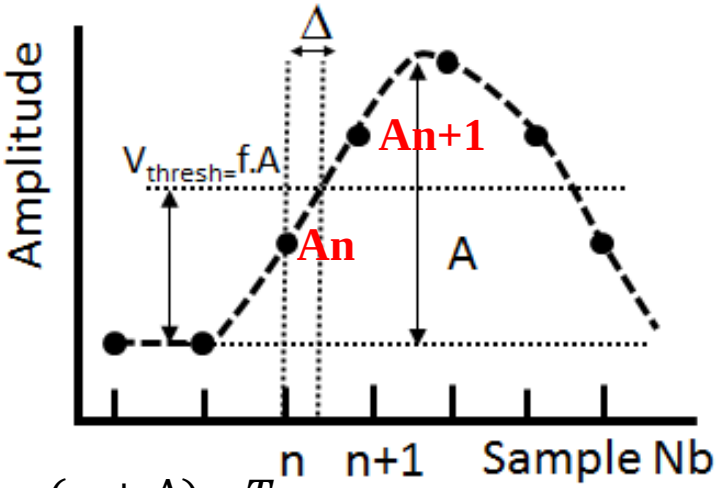
THE « WAVEFORM TDC » CONCEPT (WTDC)

WTDC: a TDC which also permits taking a picture of the real signal. This is done via sampling and digitizing only the interesting part of the signal.

Based on the digitized samples, making use of interpolation by a digital algorithm, fine time information will be extracted.





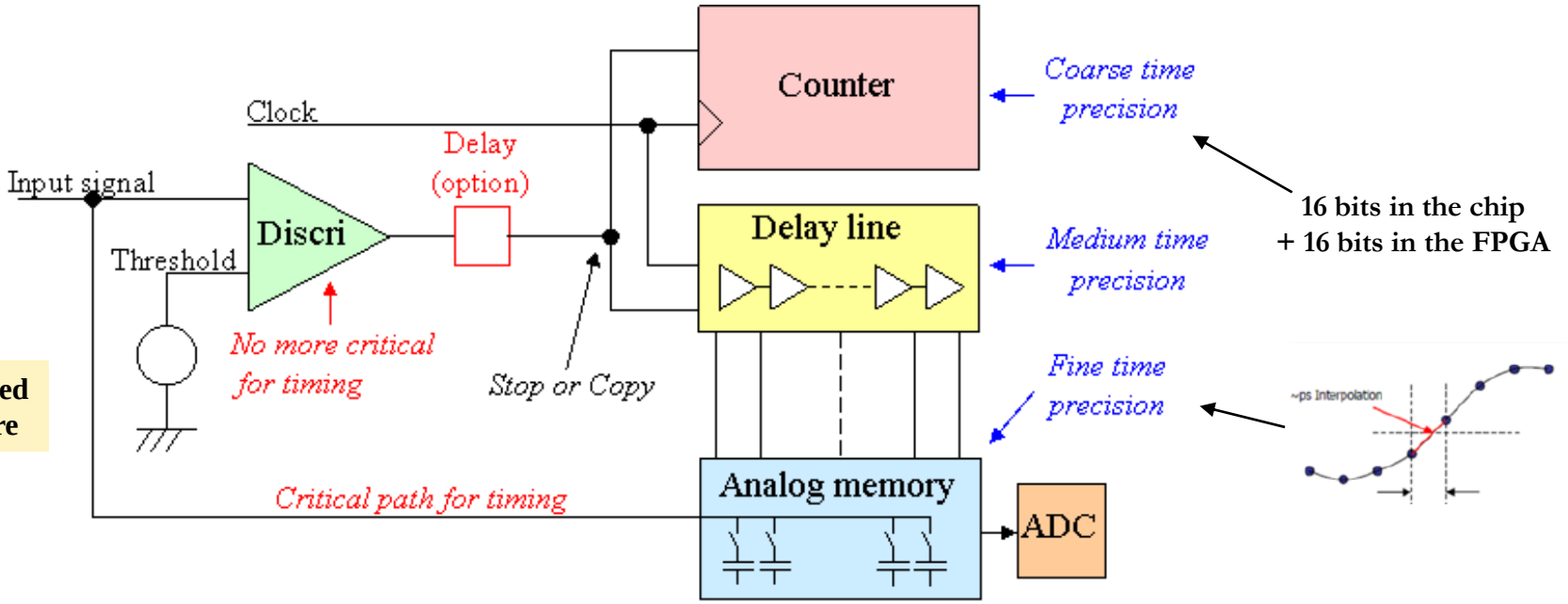
$t_0 = (n + \Delta) * T_s$

with $\Delta = \frac{f*A - A_n}{A_{n+1} - A_n}$

- **Advantages:**
  - Time resolution ~ few ps
  - No "time walk" effect
  - Possibility to extract other signal features: charge, amplitude…
  - Reduced dead-time…
- **But:**
  - waveform conversion (200 ns to 1 µs) and readout times don't permit counting rates as high as with a classical TDC

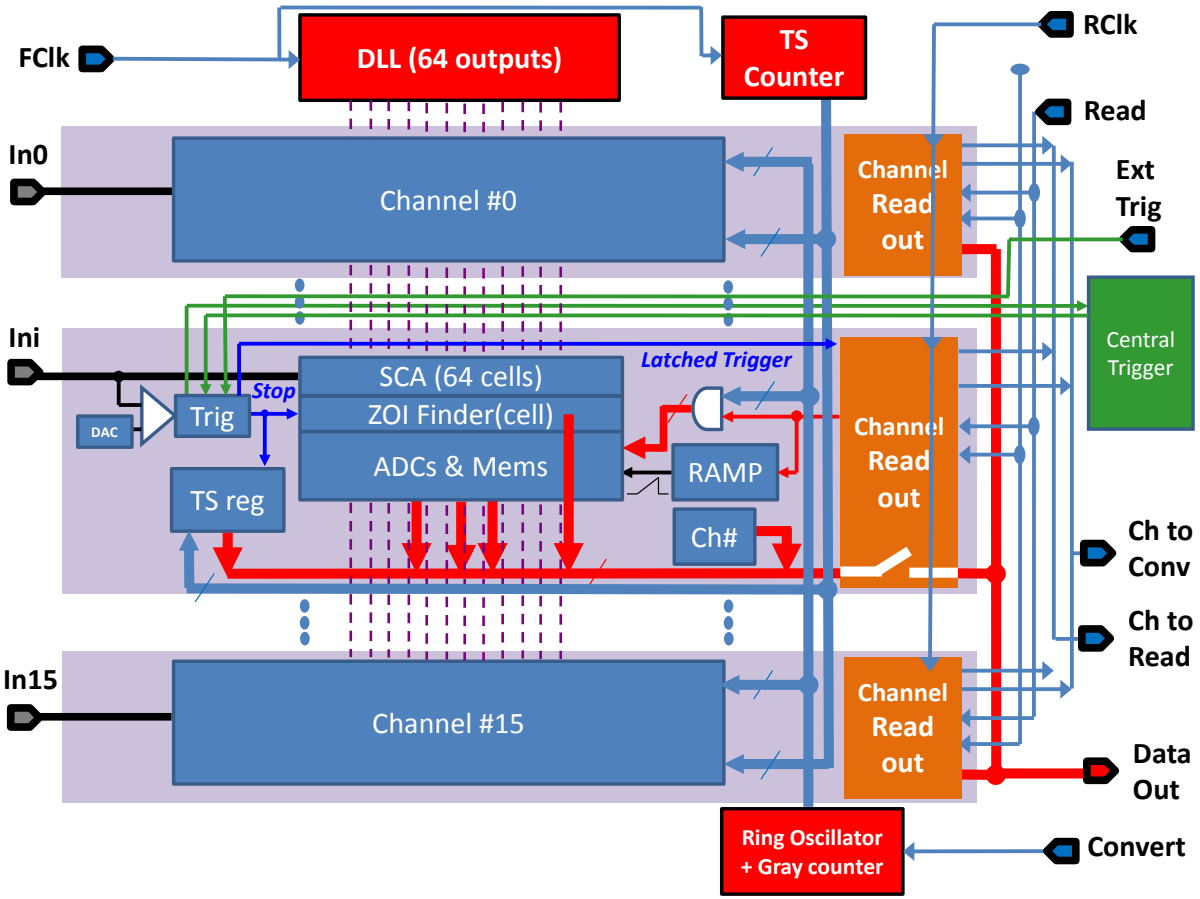
THE « WAVEFORM TDC » STRUCTURE

- The **Waveform TDC**: new concept based on **our know-how and innovating ideas**
- **Mix of DLL-based TDC and of analog-memory based Waveform Digitizer**
- Time information is given by association of contributions:
  - **Coarse** = Timestamp Gray Counter (few ns step)
  - **Medium** = DLL locked on the clock to define region of interest (100 ps minimum step)
  - **Fine** = **samples of the waveform** (**interpolation** will give a precision of a few ps rms)
- **Digitized waveform shape will give access to amplitude and charge**
- **Conversely to TDC, discriminator is used only for triggering, not for timing**



© Patented Structure

Global architecture of SAMPIC



- **One Common 16-bit Gray Counter** (FClk up to 160MHz) for **Coarse Time Stamping (TS).**

- **One Common servo-controlled DLL**: (from 0.8 to 10.2 GS/s) used **for medium precision timing & analog sampling**

- **16 independent WTDC channels each with :**
  - ✓1 discriminator for self triggering
  - ✓Registers to store the timestamps
  - ✓64-cell deep SCA analog memory
  - ✓One 11-bit ADC/ cell

  (Total : 64 x 16 = 1024 on-chip ADCs)

- **One** common 1.3 GHz oscillator + counter used as timebase for all the **Wilkinson A to D converters.**

- **Read-Out interface: 12-bit LVDS bus running at > 160 MHz (2 to 4 Gbits/s)**
- **SPI Link** for Slow Control

A LITTLE BIT OF HISTORY

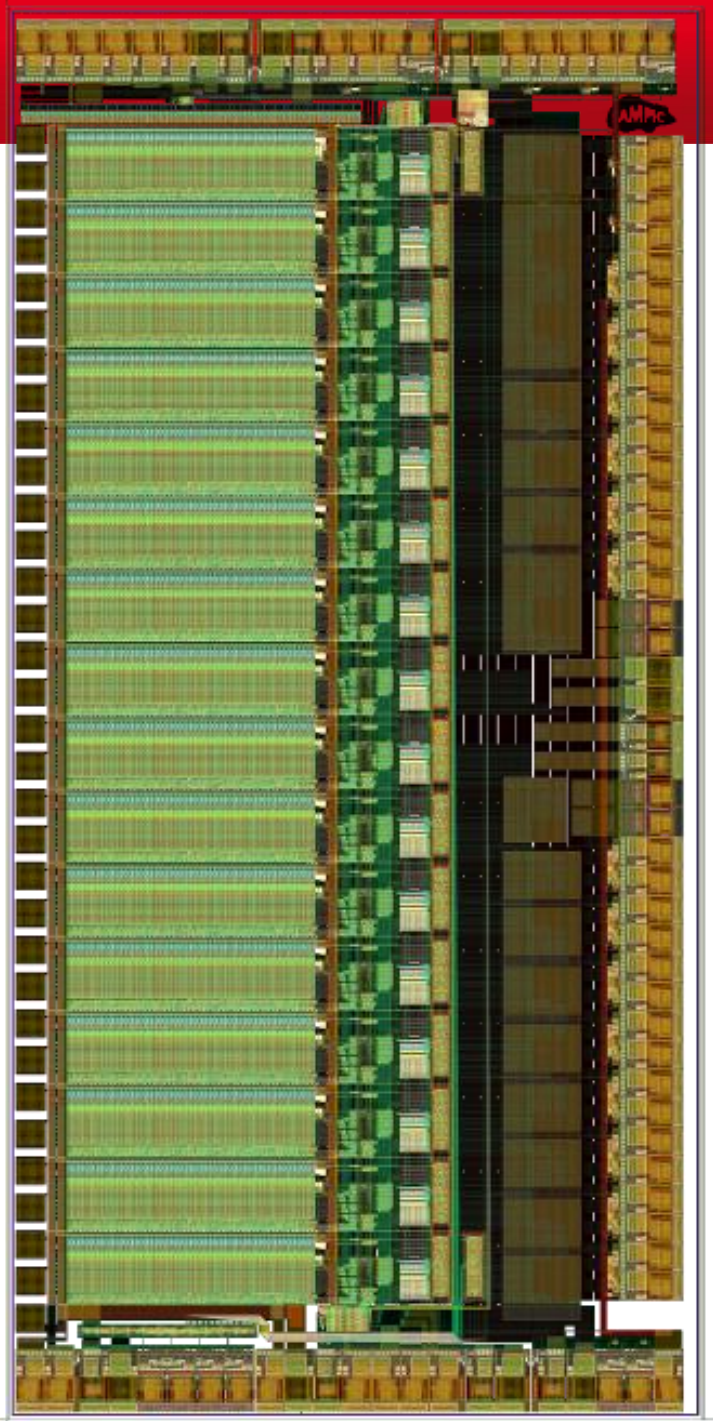
- **SAMPIC_V0 was submitted in February 2013. Its tests started in July 2013. It clearly validated the concept but a few bugs were found.**

- **SAMPIC_V1 corrected all the (little) problems from V0 and was submitted in November 2014. It was considered as releasable to users end of 2015.**
- **This is the baseline version currently used by different teams (CEA, CERN, Univ of Kansas, CMS/TOTEM, ATLAS, SHiP, PANDA, …) for their test benches or detectors (PMTs, MCPPMTs, APDs, SiPMs, fast Silicon Detectors, Diamonds, …)**

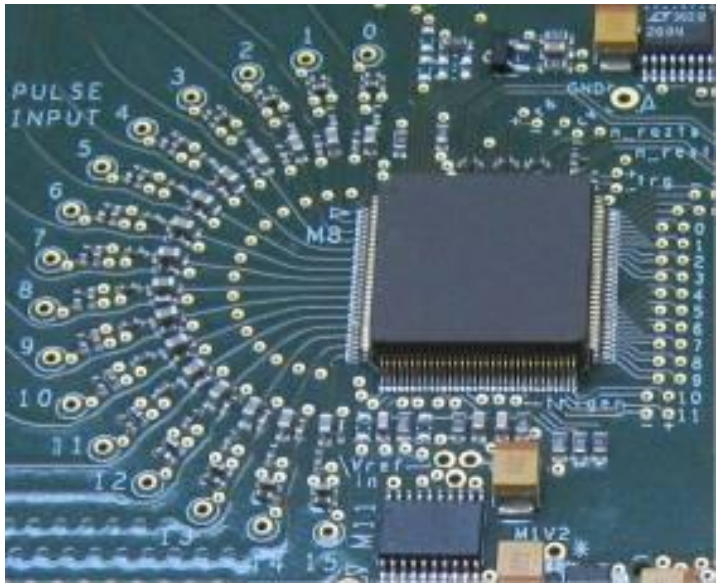
- **We got a lot of feedback concerning the chip, the module and the software. A raising point was that it was more urgent to improve the system aspects than to concentrate on the already good time resolution.**

- **We thus mostly worked since on performing many improvements on digital blocks (ASIC & FPGA) and software.**

SAMPIC_V1

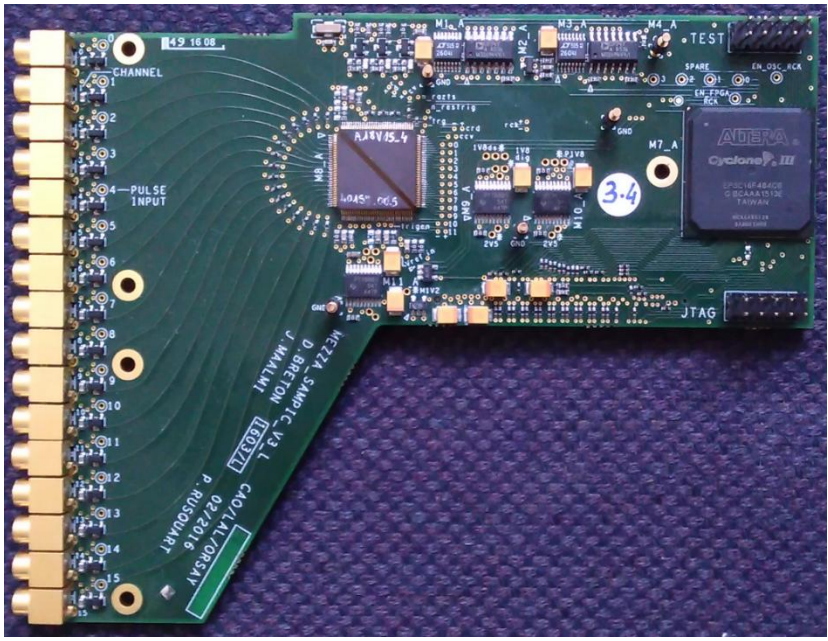


- Technology: **AMS CMOS 180nm**
- Surface: 8 mm^2
- Package: QFP 128 pins, pitch of 0.4mm



SAMPIC MODULE & ACQUISITION SETUP

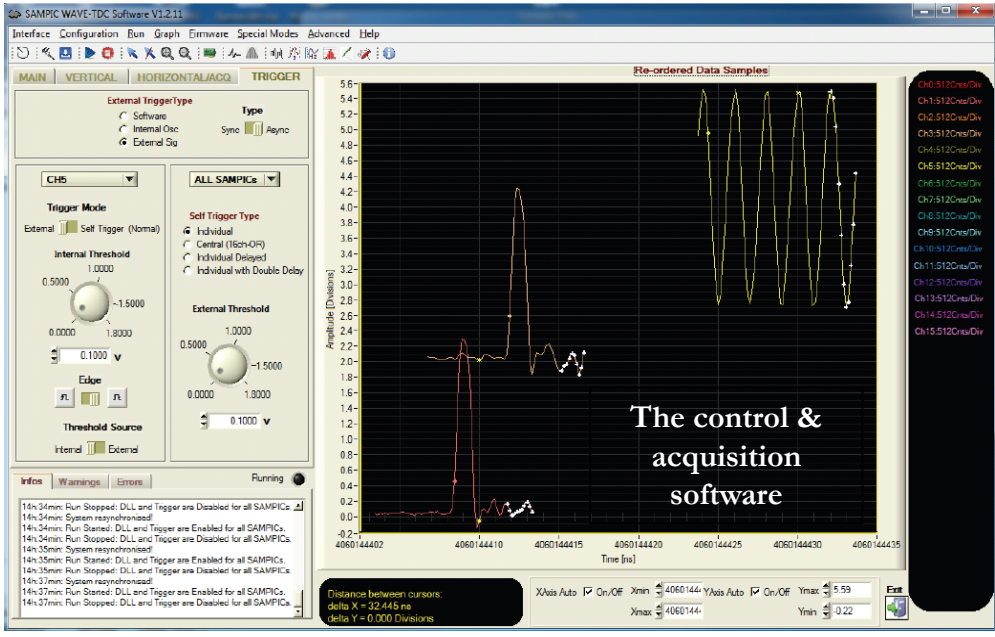
- 32-channel module integrating 2 mezzanines
- 1 SAMPIC/mezzanine, 3 layers of boards
- **Fully designed and cabled at LAL**
- USB, Gbit Ethernet UDP (RJ45 & Optical)



- **Acquisition software** (& soon C libraries)

=> full characterization of the chip & module

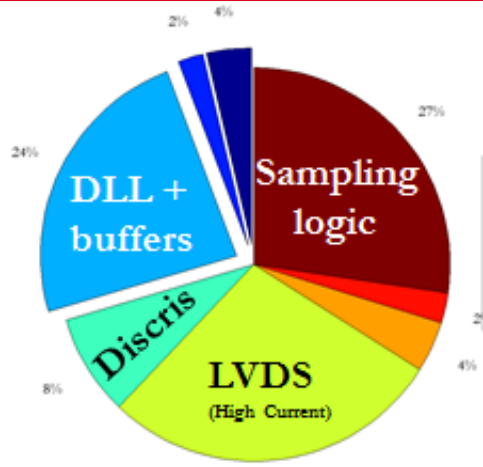
- Timing extraction (dCFD, interpolation…)
- **Special display** for **WTDC mode**
- Data saving on disk.
- Used by all SAMPIC users.



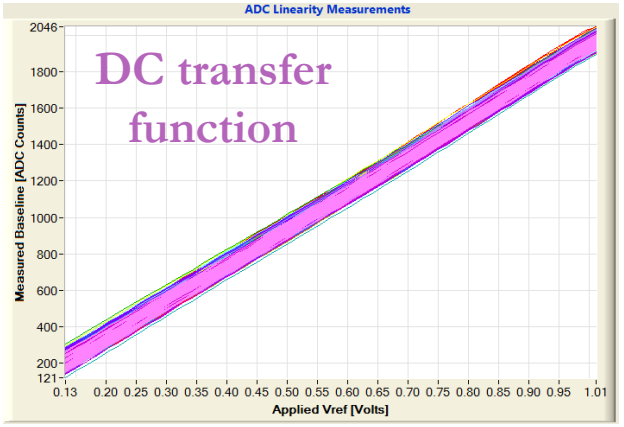
SAMPIC_V1 PERFORMANCES

- Power consumption: **10mW/channel**
- 3dB bandwidth > **1 GHz**
- Discriminator noise ~ **2 mV rms**
- Counting rate **> 2Mevts/s** (full chip, full waveform), up to 10 Mevts/s with Region Of Interest (ROI)

Power distribution

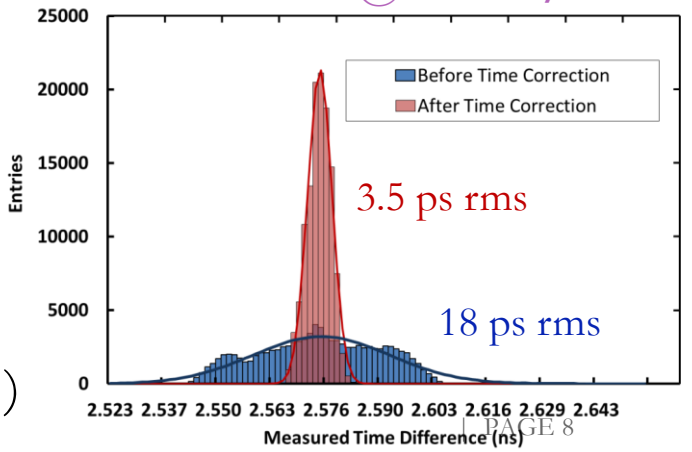


- Wilkinson ADC works with internal **1.3 GHz** clock
- Dynamic range of **1V**
- Gain dispersion between cells ~ **1%** rms
- Non linearity **< 1.4 %** peak to peak
- After correction of each cell (linear fit): noise = **0.95 mV rms**



- Time Difference Resolution (TDR):
- Raw non-gaussian sampling time distribution due to DLL non-uniformities (TINL)
- Easily calibrated & corrected (with our sinewave crossing segments method [D. Breton&al, TWEPP 2009, p149])

Ex: TDR @ 6.4 GS/s



NEW VERSIONS SINCE SAMPIC_V1

- Intermediate version of the chip submitted in November 2015: SAMPIC_V2
  - Introduction of many new blocks and functionalities
- After the tests of V2 and the feedback from a few beta-users, a new version (SAMPIC_V3) was submitted in November 2016.
  - Correction of the few problems found in V2 (limited bandwidth, …) and introduction of other new blocks and functionalities
- SAMPIC_V3 came back in April 2017, and showed a huge over consumption on one power pin (200 mA vs a few mA)
  - After a few weeks of investigation, we finally identified the default.
  - It couldn't be seen by simulation.
  - However, the chip was functional but obviously not with the nominal performance (local voltage drifts due to high currents, extra delays …). We could thus check that all the new functionalities were operational.

Thermal view

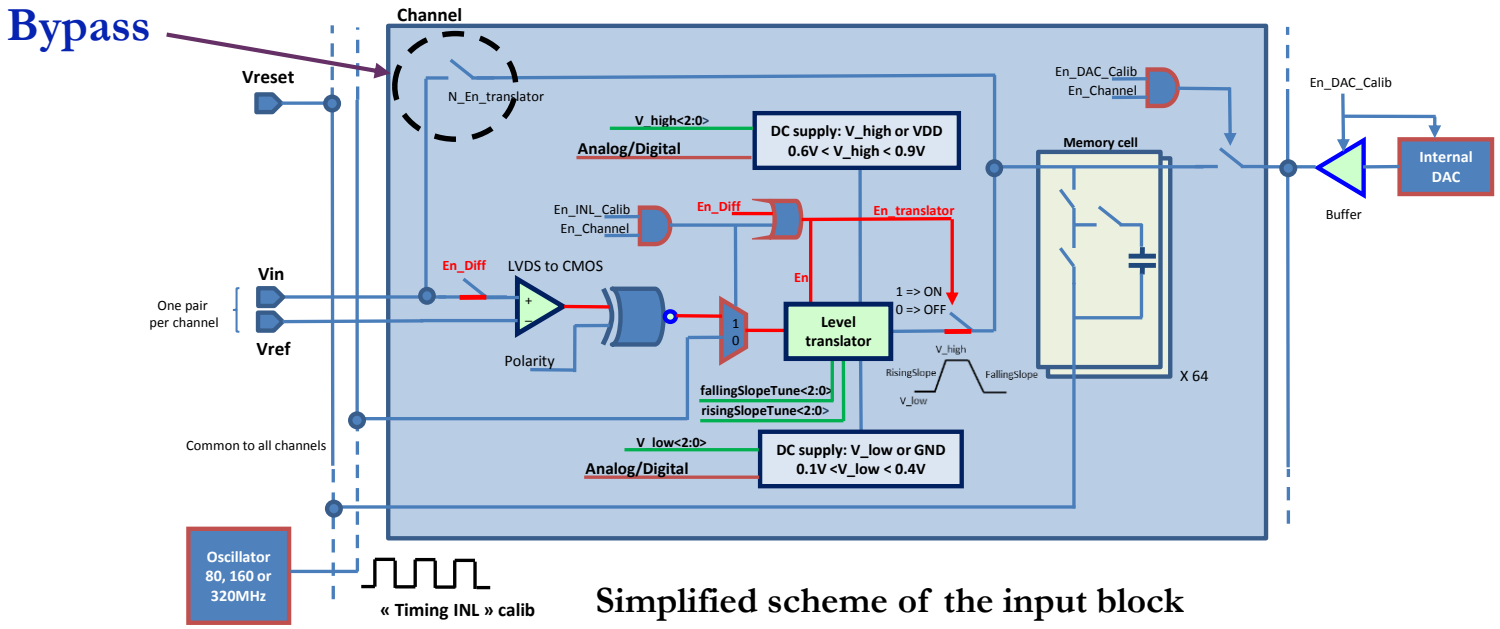
- The chip was corrected and submitted in early June 2017
  - But … technology manufactured by AMS instead of IBM (equivalent to Canadian vs French) => numerous adaptations required…
  - The new chip came back end of November 2017.

NEW FEATURES IN SAMPIC_V3

- **All DACs necessary for controlling the chip have been integrated**
- **Wider sampling frequency range (0.8 GS/s to 8.5 GS/s)**
- **Coarse timestamp extended to 16 bits**
- **Addition of input block both to deal with differential digital signals ("SAMPET" option) & to perform standalone calibrations**
- **Dual row of input pads** => permits keeping the possibility of direct analog access for ultimate time precision and testability
- **Auto-conversion mode for ADC (channel conversions are independent) but conversion can also be driven from outside, which permits building a two-level trigger based on many chips for a common event selection.**
- **Improved "central trigger" (multiplicity of 1, 2, or 3) with possibility of common deadtime & smart channel selection**
- **Improved PostTrig**
- **ADC resolution internally selectable in the range 7 to 11 bits**
- **Individual integrated TOT measurement + Trigger Filter based on TOT**
- **"Ping-Pong" (toggling) mode: channels can work in pairs.**
- **Channel chaining option**: user-defined sets of channels can be chained in time.
- …

NEW INPUT BLOCK OF SAMPIC

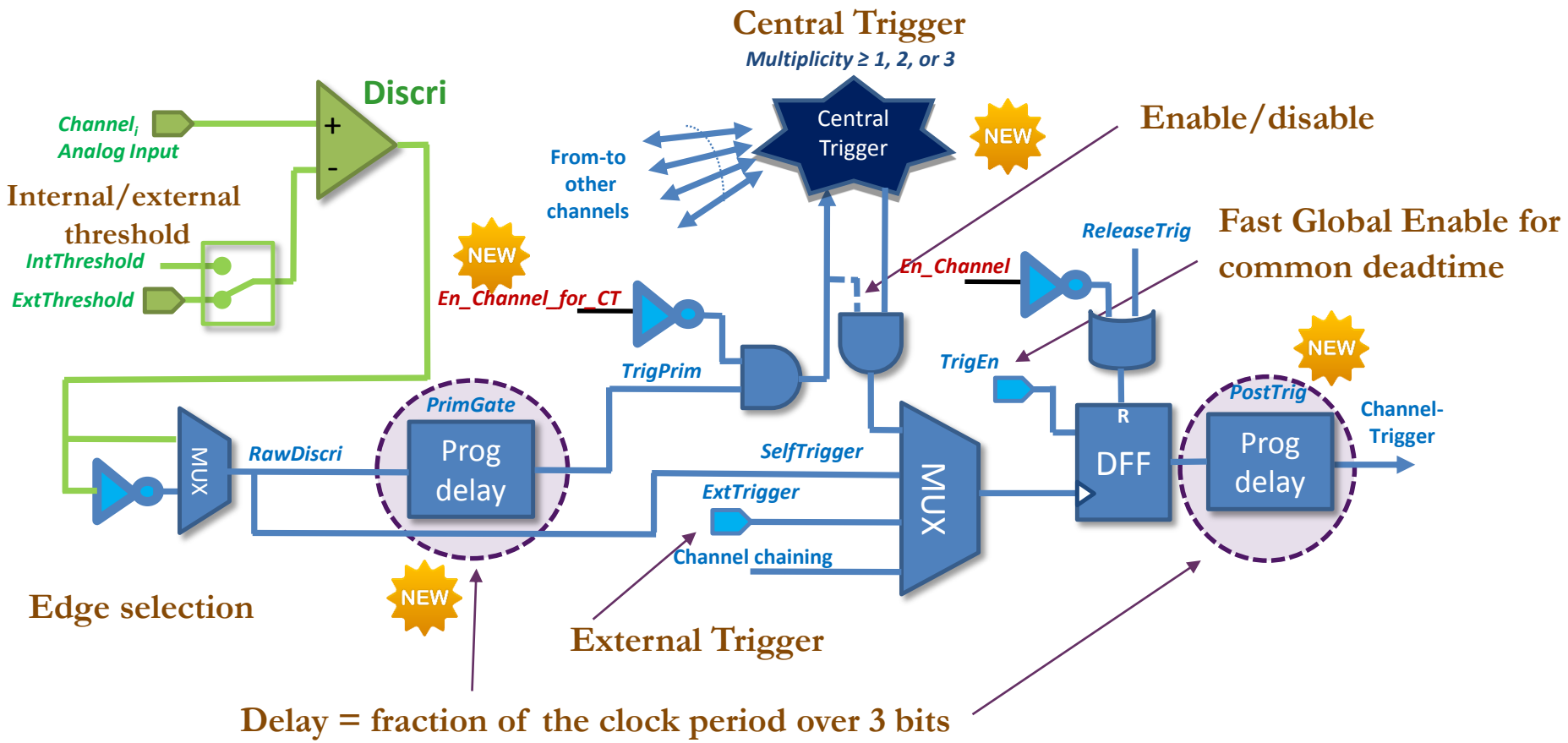
- Translator input block : input signal can feed the memory directly (Bypass Mode) or pass through the translator
- It permits among others:
  - Self calibration of the chip
  - Compatibility with (small amplitude) digital differential signaling
- Gives the possibility of an autonomous time calibration for integrated systems
- Fixed amplitude at translator output => only a few samples (ROI) and fast conversion (≤ 8 bits) => behaves like a TDC



Simplified scheme of the input block

NEW TRIGGER SCHEME

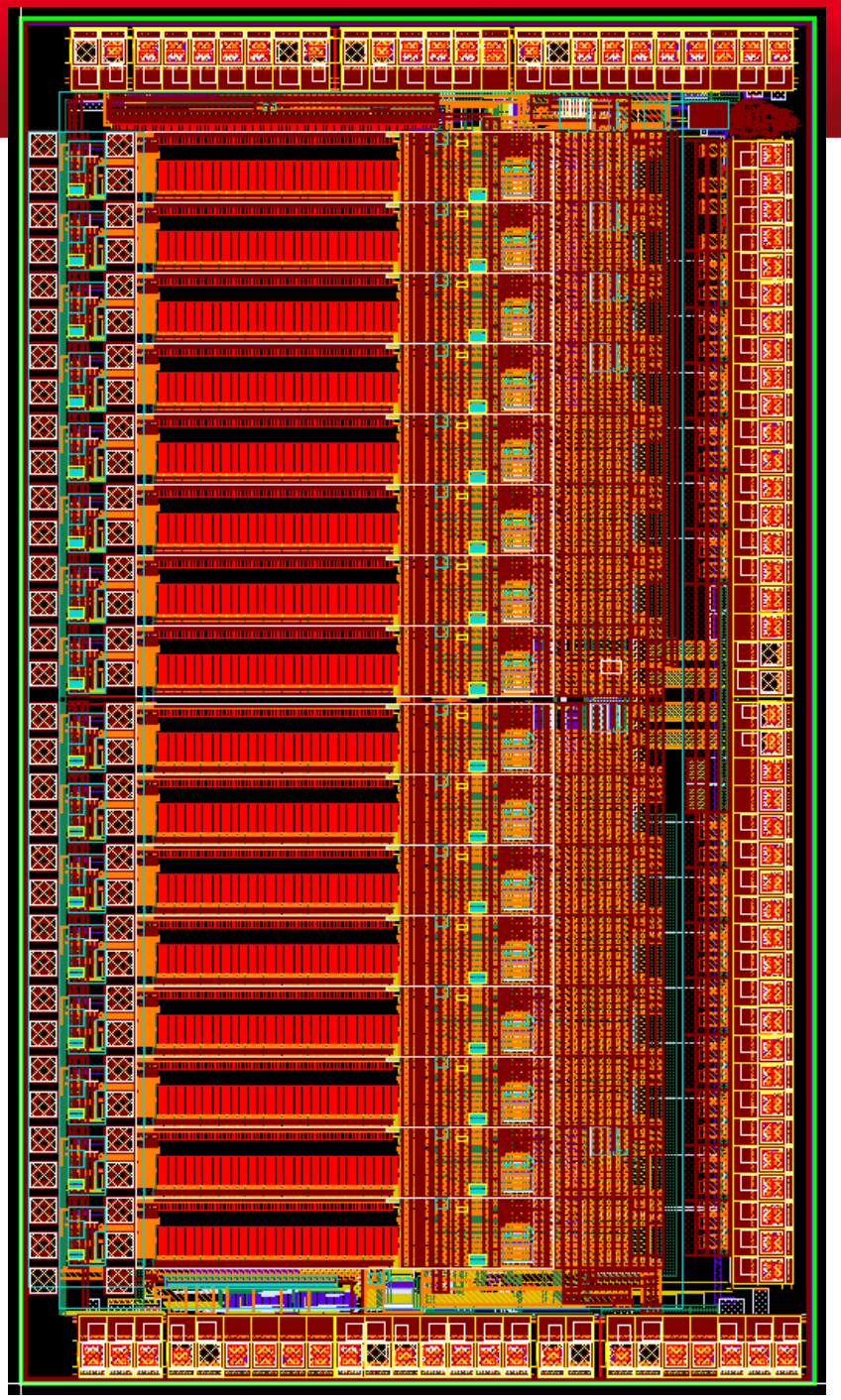
- One very low power signal discriminator/channel
- One 10-bit DAC/channel to set the threshold (which can also be external)
- Several trigger modes programmable for each channel:



⚠ Only the triggered channels are in dead time

SAMPIC_V3 LAYOUT

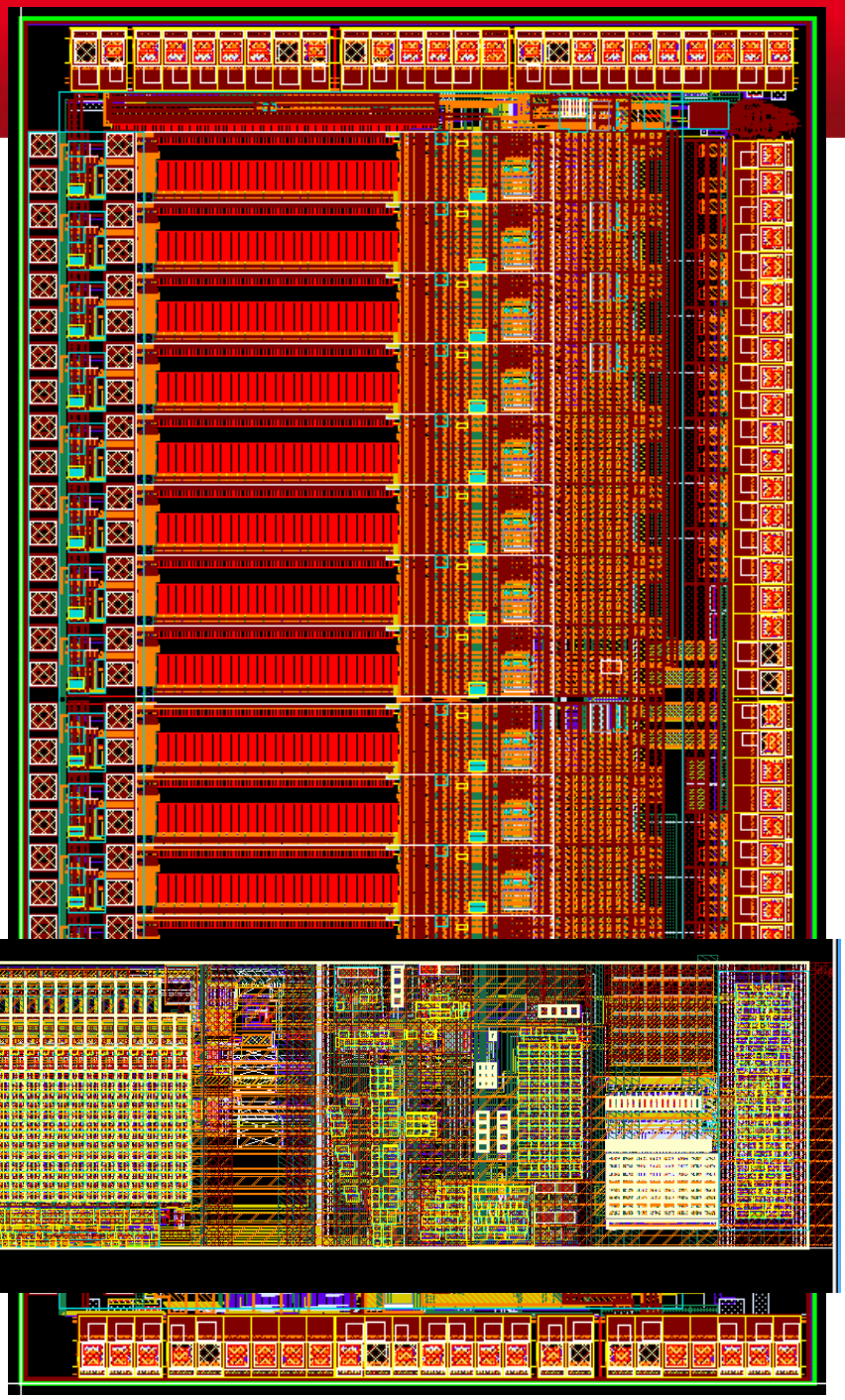
- **Double raw of pads**:
  - External row: standard cabling for usual applications where translator stage can be used and self calibration performed
  - Internal row: for optimal bandwidth, time precision and testability
- Still one NC pin... but on the hedgehog !

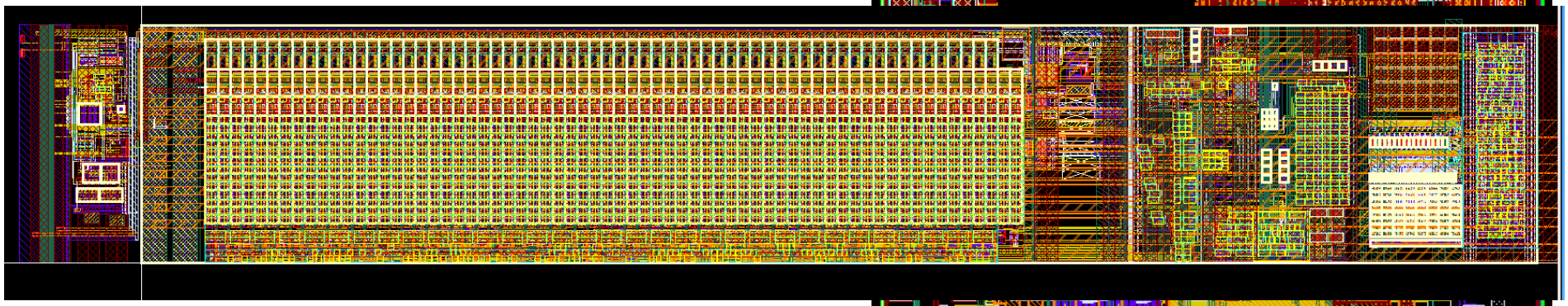


SAMPIC_V3 LAYOUT

- **Double raw of pads**:
  - External row: standard cabling for usual applications where translator stage can be used and self calibration performed
  - Internal row: for optimal bandwidth, time precision and testability
- Still one NC pin... but on the hedgehog !

• Dimensions of a channel: 200µm x 1.3mm



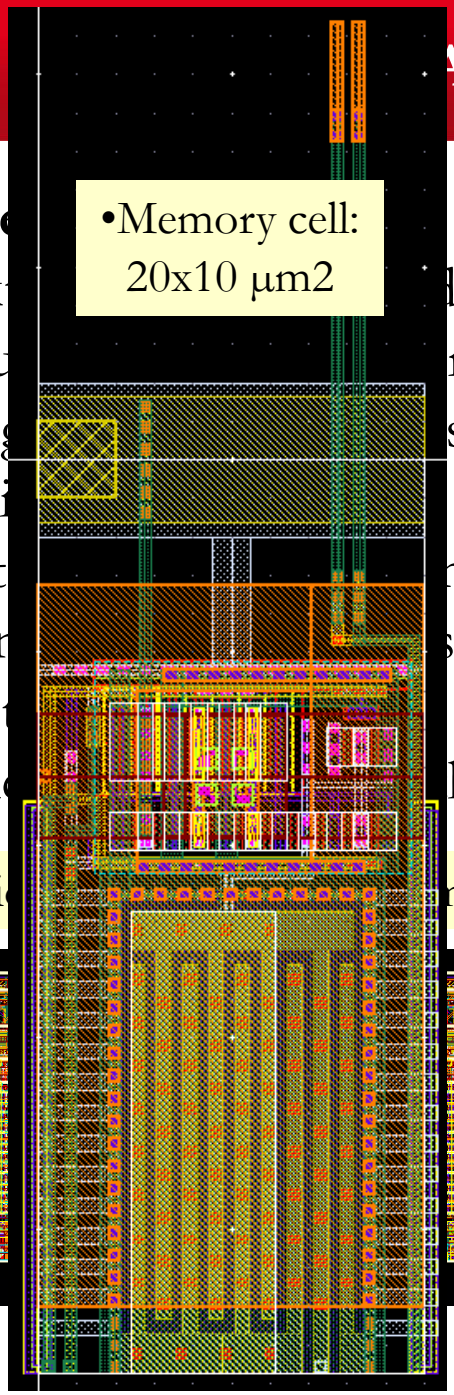


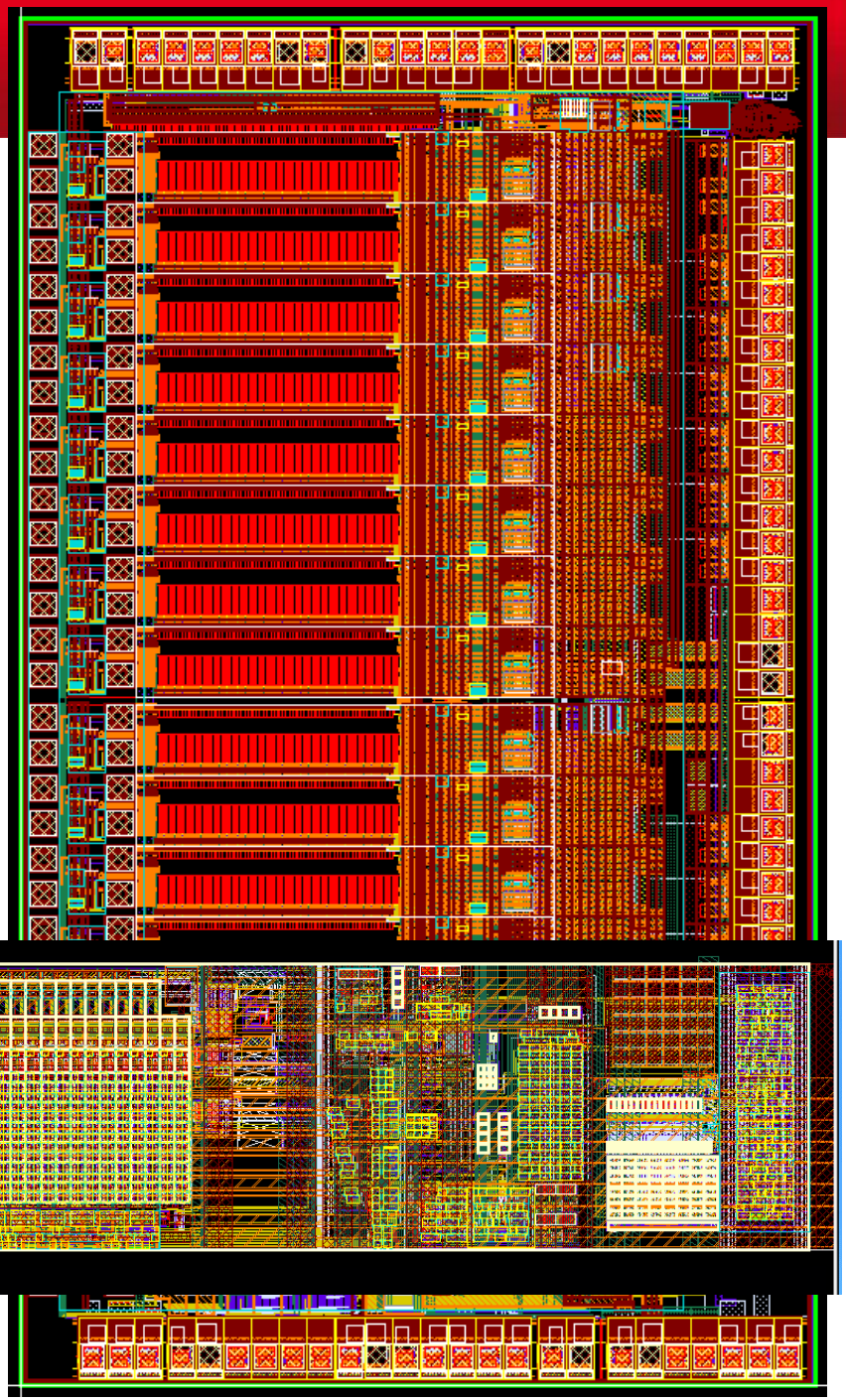
AYOUT

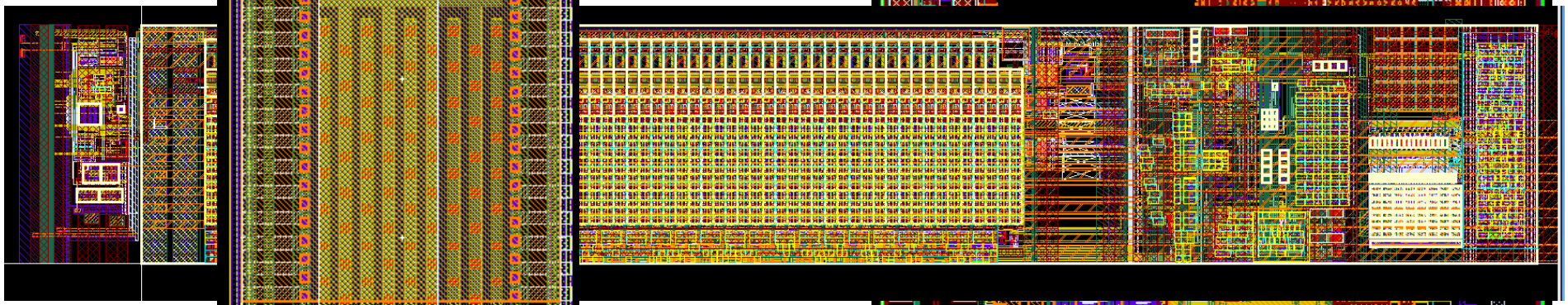
- **Double**
  - Ex… l cabling for usu… re translator sta… self cali…
  - Int… nal bar… sion and test…
- Still on… he hedgehog !

• Memory cell: 20x10 µm2

• Dimensi… n x 1.3mm

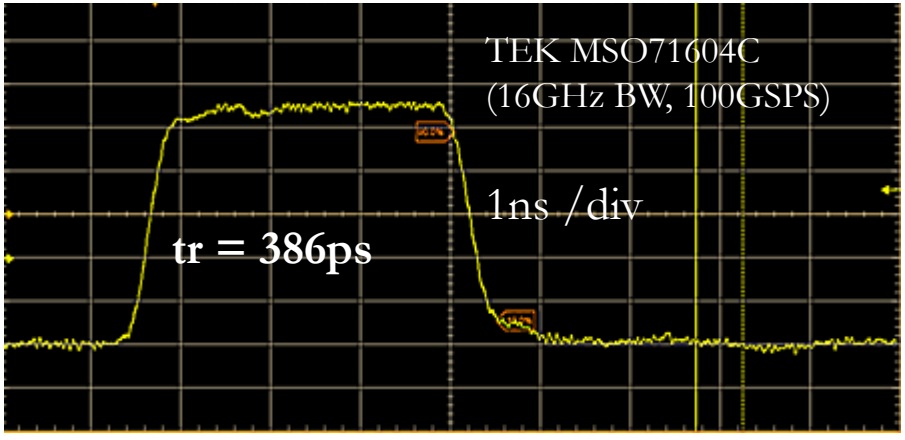


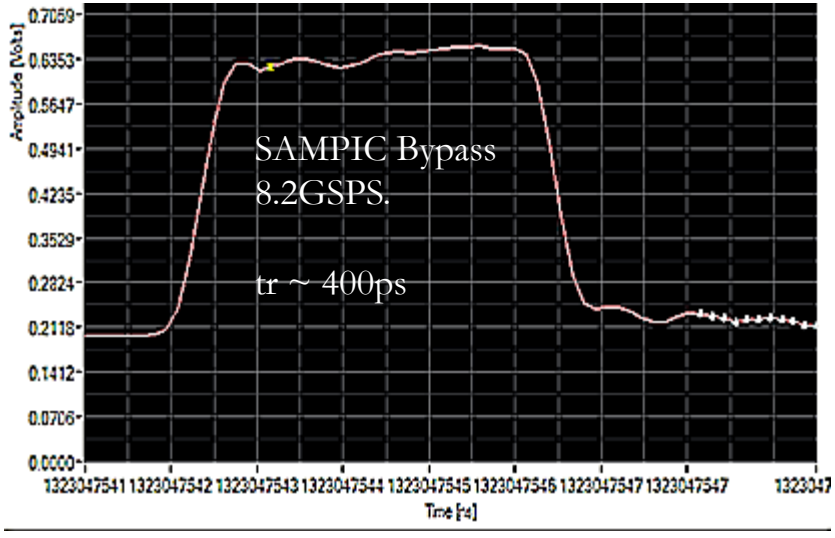


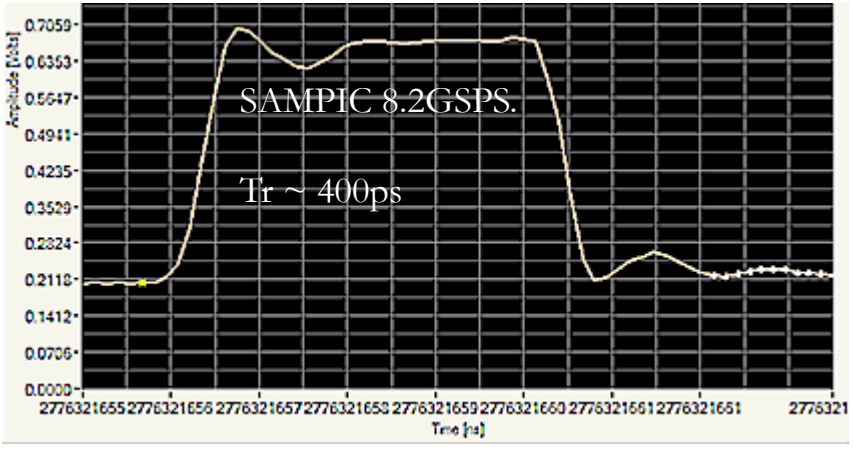


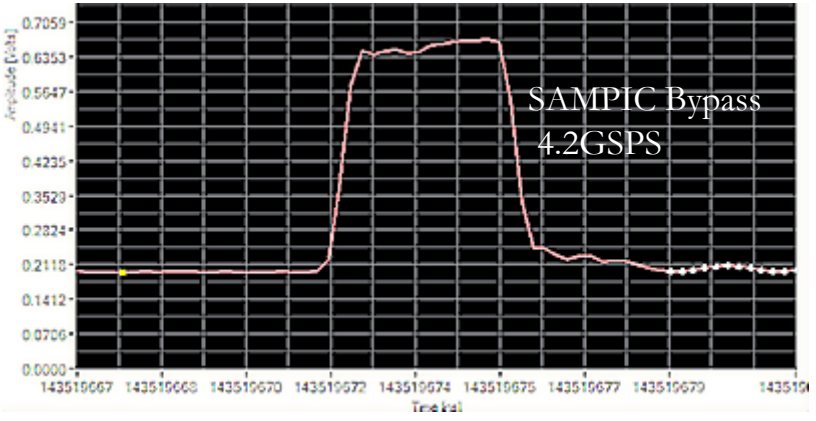
WAVEFORM RESPONSE

- **We send a pulse (~460 mV pp) with very sharp edges and compare the response from SAMPIC and from a high-end oscilloscope:**
  - Signal produced by a LeCroy 9214 generator.
  - Permits estimating **SAMPIC bandwidth: > 1 GHz**



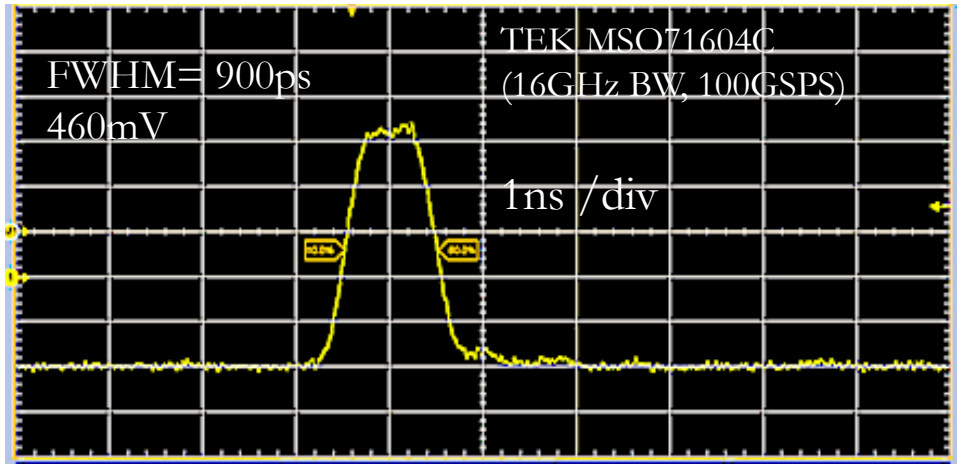


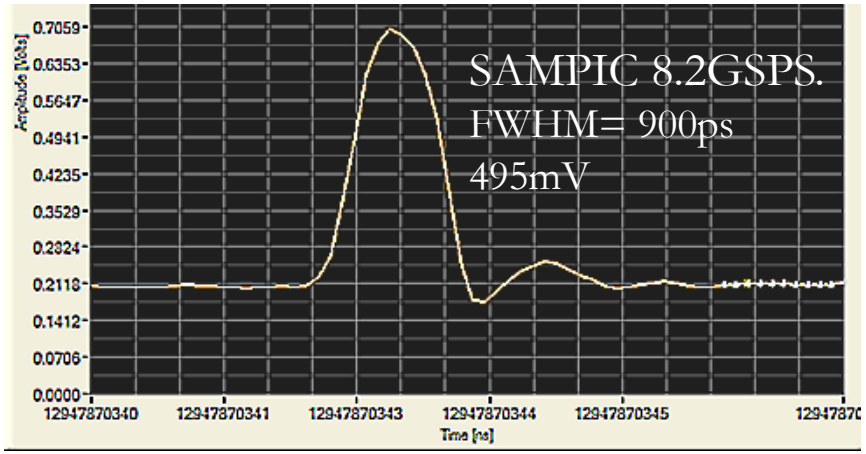


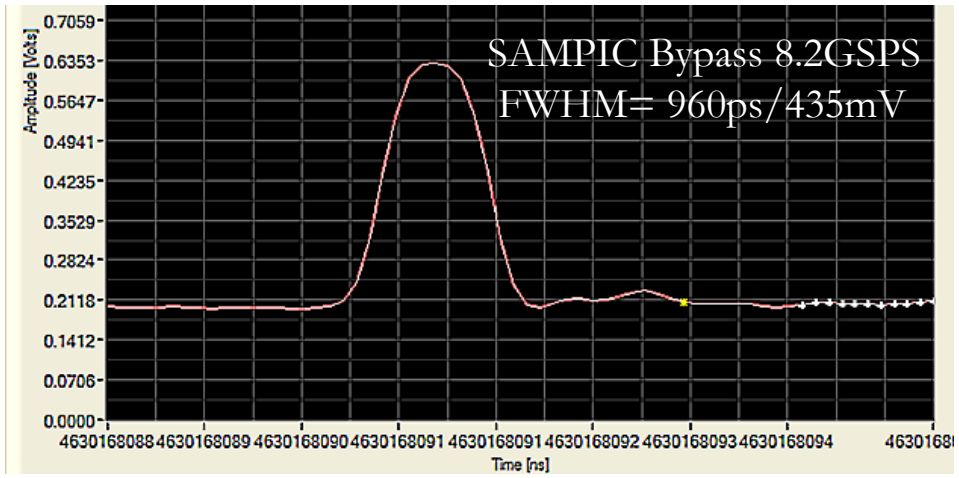


SHORT SIGNAL RESPONSE

Lecroy 9214 signal with 900 ps width





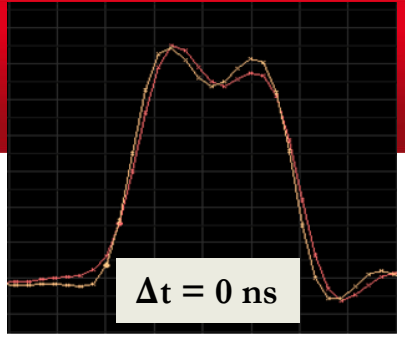


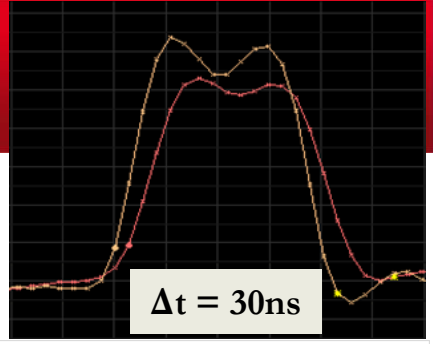
TIME RESOLUTION

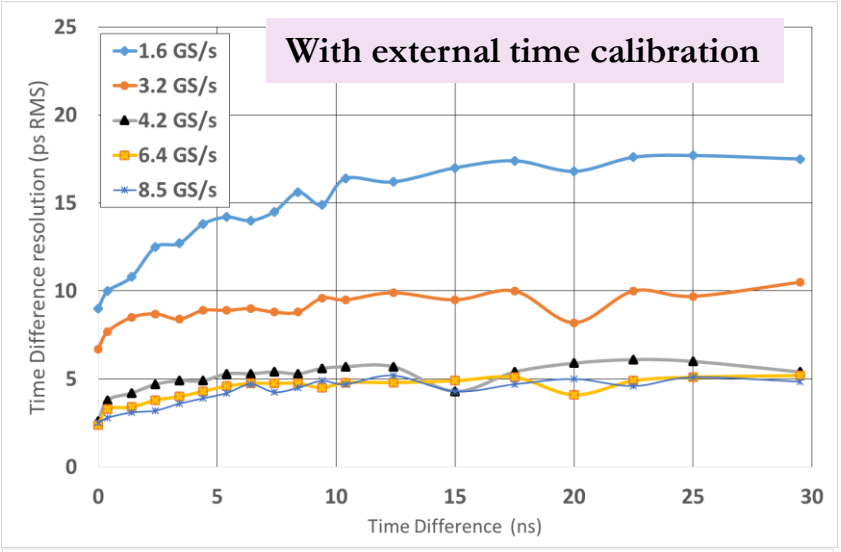
- The new DLL has been re-worked for improving the resolution for the lower sampling frequencies
- Delays have to be made by a cable box => rise time degrades with delay …

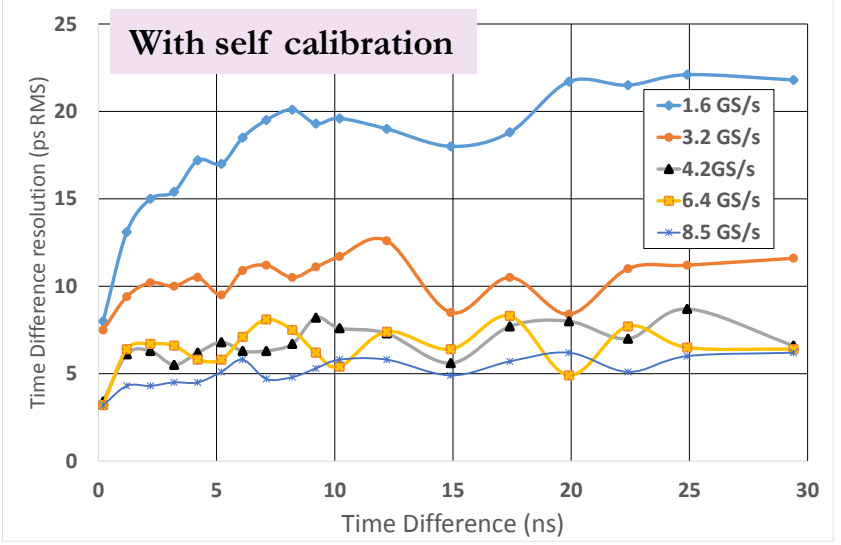
- SAMPIC can be time-calibrated with external signals
  - A **TDR of ~5 ps rms** is achieved between 4.2 and 8.5 GS/s
  - The TDR remains below 10 ps rms for 3.2 GS/s and below 18 ps rms for 1.6 GS/s

- But calibration can also make use of internally generated signals (self-calibration)
  - Limited jitter degradation (~20%)
  - Permits integration in detectors…



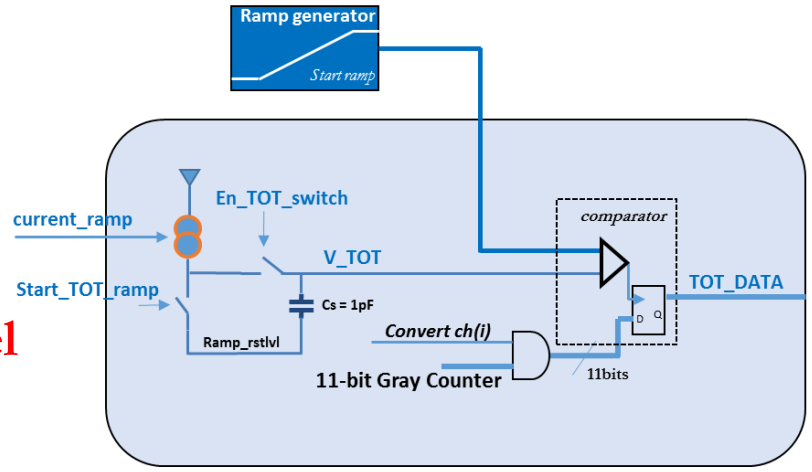


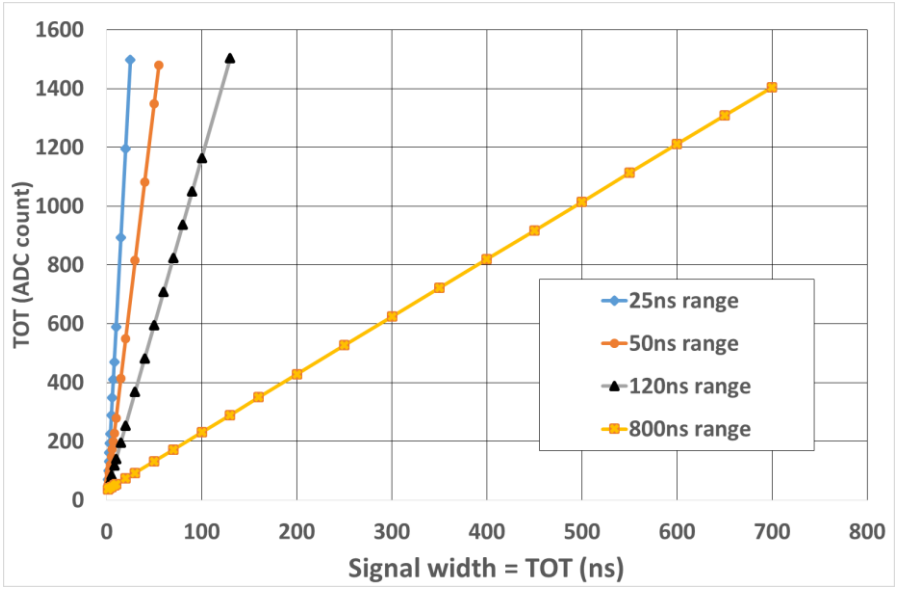


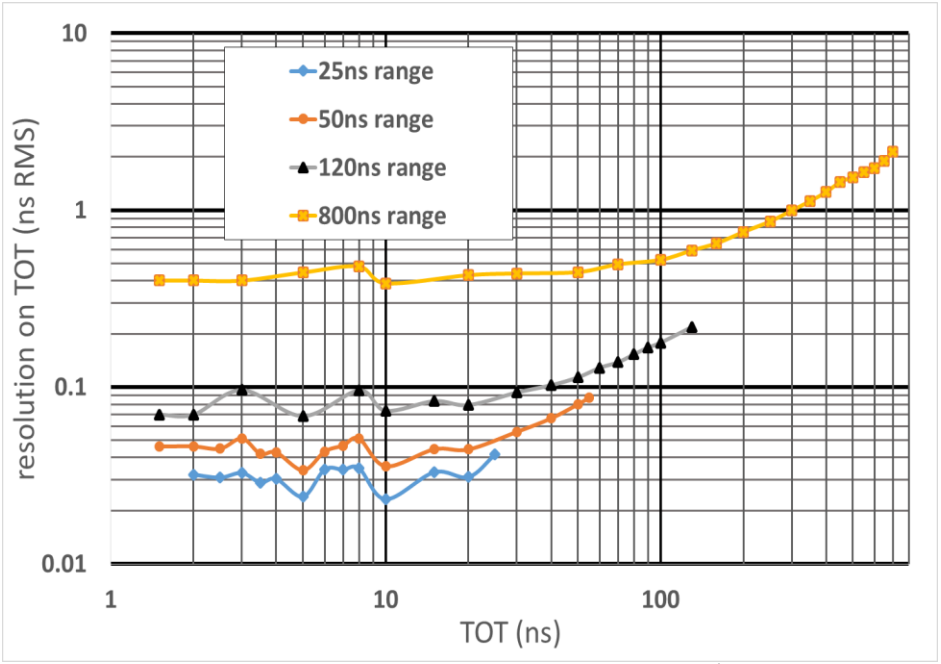


NEW FEATURES: TOT MEASUREMENT

- SAMPIC is tailored for digitizing a short signal or only a small part of a longer one (eg rising edge) to extract the timing.
- In SAMPIC_V3: addition of a ramp TimeAmplitudeConverter for each channel seen as a 65th memory cell during digitization => >10bit TOT TDC



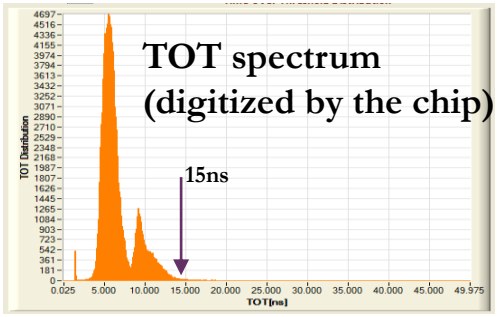


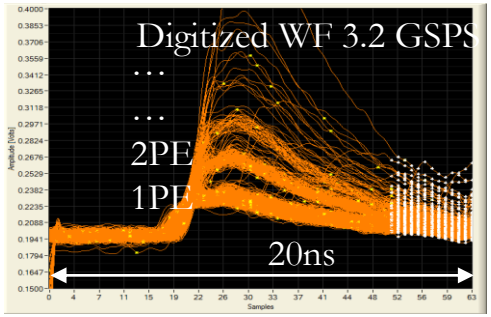


Measurement ranges between 2 and 700 ns.

NEW FEATURES: ON-CHIP TOT FILTER

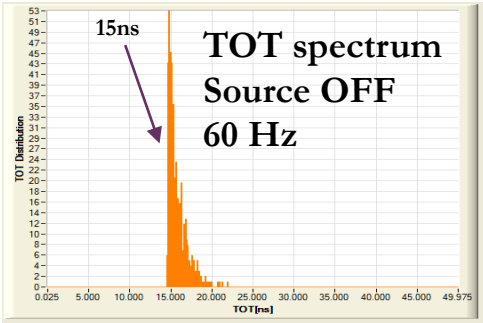
- **Rejects triggered signals with TOT < programmable value** (2 -700 ns range)
- **Many possible applications including rejection of noise of SiPM coupled to crystals (here KETEK SiPM + PbWO4 + Na Source, @ 20°C, *courtesy of S. Shaarvy, CEA/Irfu*)**
  - Th= 20 mV (0.5 PE), TOT_Filter OFF, **700 kHz** rate (of digitized events)

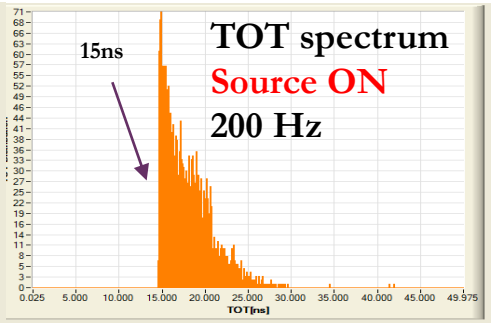


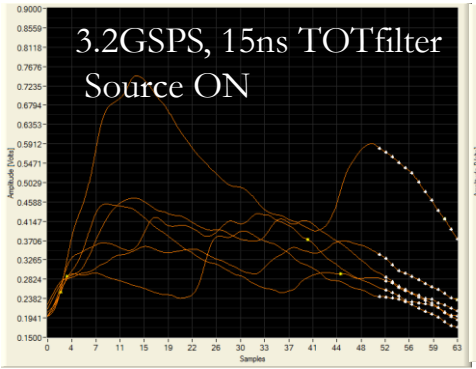


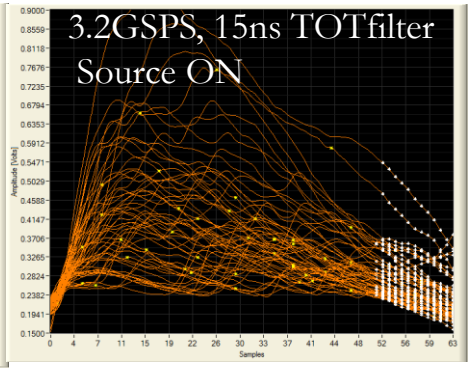
SiPM: KETEK PM3350TP-SB0
3x3 mm², 50µm pitch, trench design,
Operation @ 29V (2.5V overvoltage)

  - Th= 50 mV (1.25 PE), TOT_Filter OFF => **60 kHz** rate (unfortunately, the TOT spectrum has been lost…)
  - Th= 50 mV (1.25 PE), TOT_Filter ON = **15ns** => **rate decreased by a factor 300**



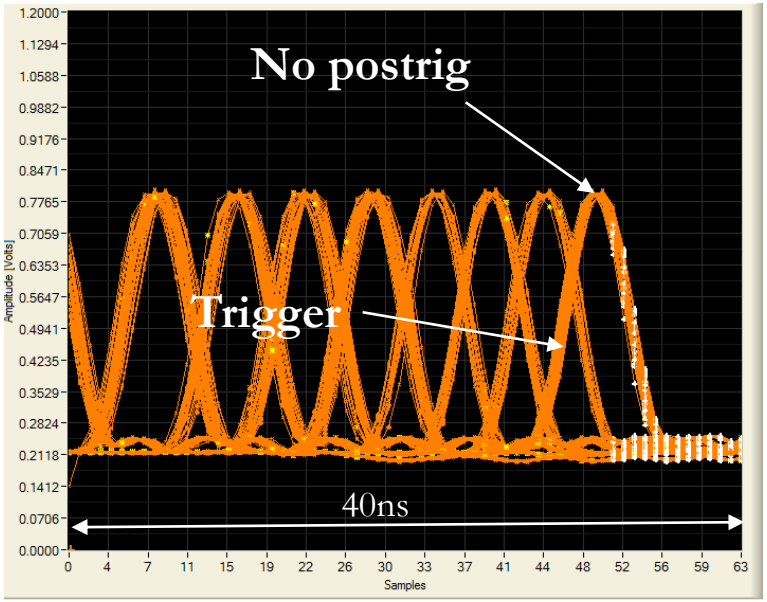






NEW FEATURES: PROGRAMMABLE POSTTRIG

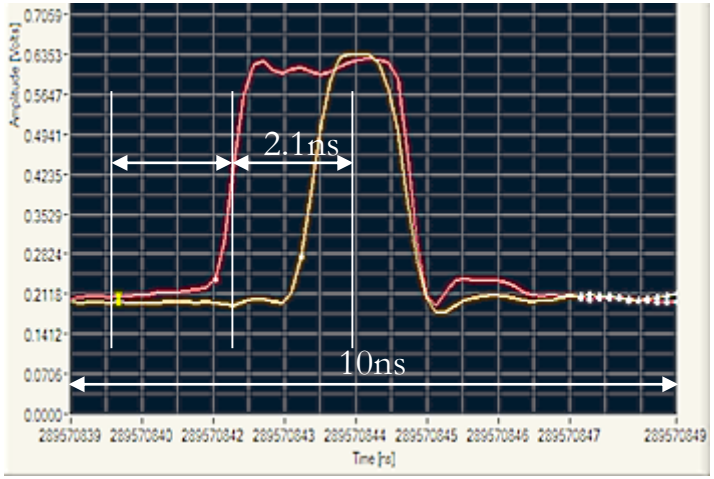
- Allows to "move the signal" by fractions of the acquisition window
  => oscilloscope-like PostTrig
- **8-step (~linear) programmable asynchronous delay that must be proportionnal to the sampling frequency**
- Mostly useful for low sampling frequencies
- Very **compact delay-locked** loop system also reused for 3 other purposes in each channel



Effect of the 8 posttrig values (1.6 GSPS)

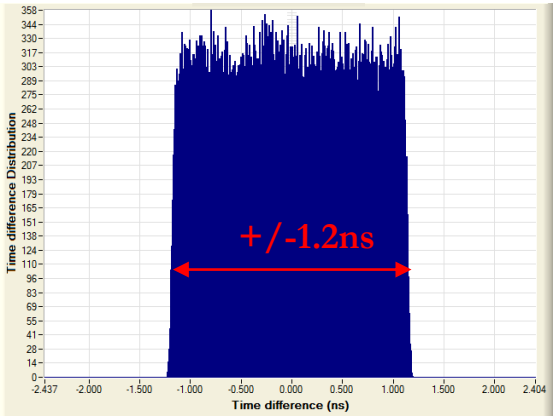
NEW FEATURES: CENTRAL TRIGGER/ COINCIDENCE

- Each channel can be triggered by the CENTRAL TRIGGER: can be the **OR, or a Coincidence of ≥ 2 or ≥ 3 channels**
- Coincidence Gate generated by an asynchronous delay as previously described.
- **Only 1ns of extra latency on trigger decision**
- Test below using 2 signals (>> 1MHz) with random phases sent to 2 channels with 1.2 or 2.1ns coincidence gate.

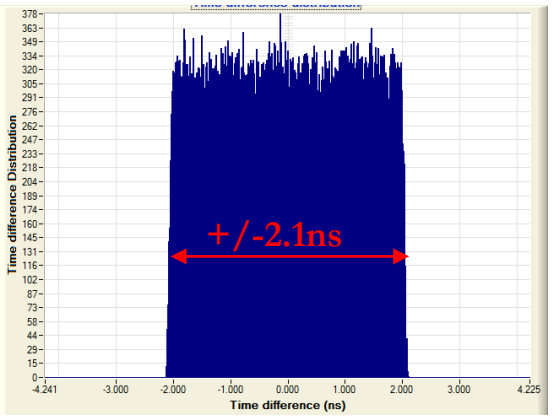


1 of the couples of signals digitized. 2.1 ns gate @ 6.4GSPS

TimeDifference histogram (from the digitized waveform)



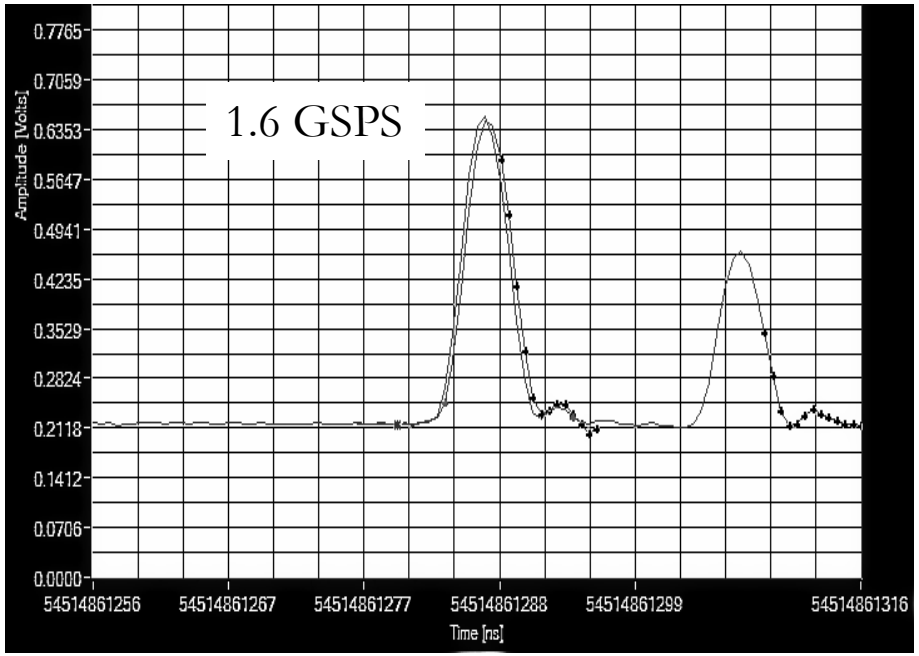
« 1.2ns » coincidence gate



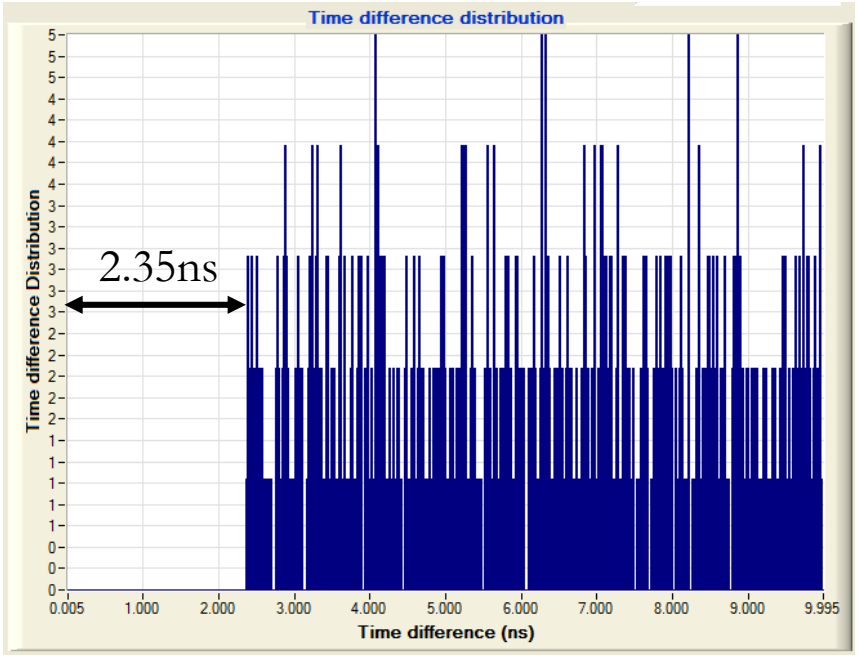
« 2.1ns » coincidence gate

PING-PONG MODE

- **PING-PONG**: use alternatively 2 SAMPIC channels, connected or not to the same source, to reduce the dead time and allow double or conditionnal pulse detection.
- Min re-triggering distance : 2.35 ns (see below)
- Drawback: number of channels divided by a factor 2 if source is common



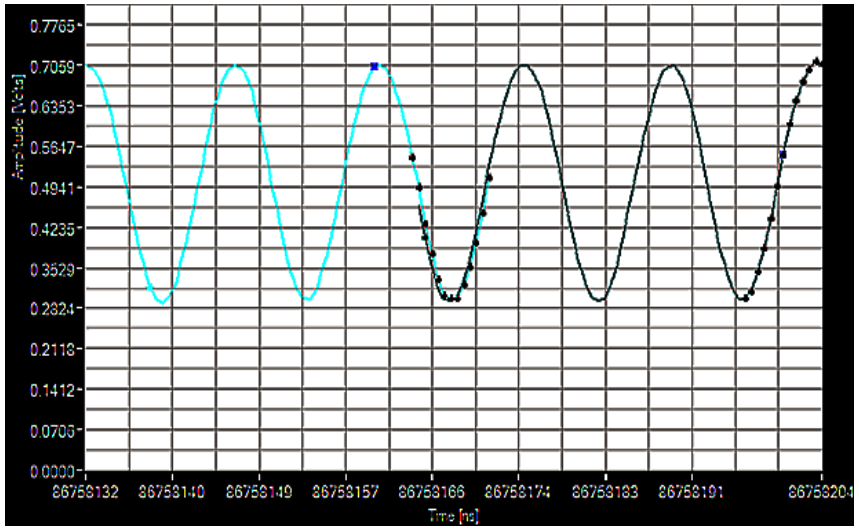
1st pulse recorded on channel 2
2nd pulse recorded on channel 3



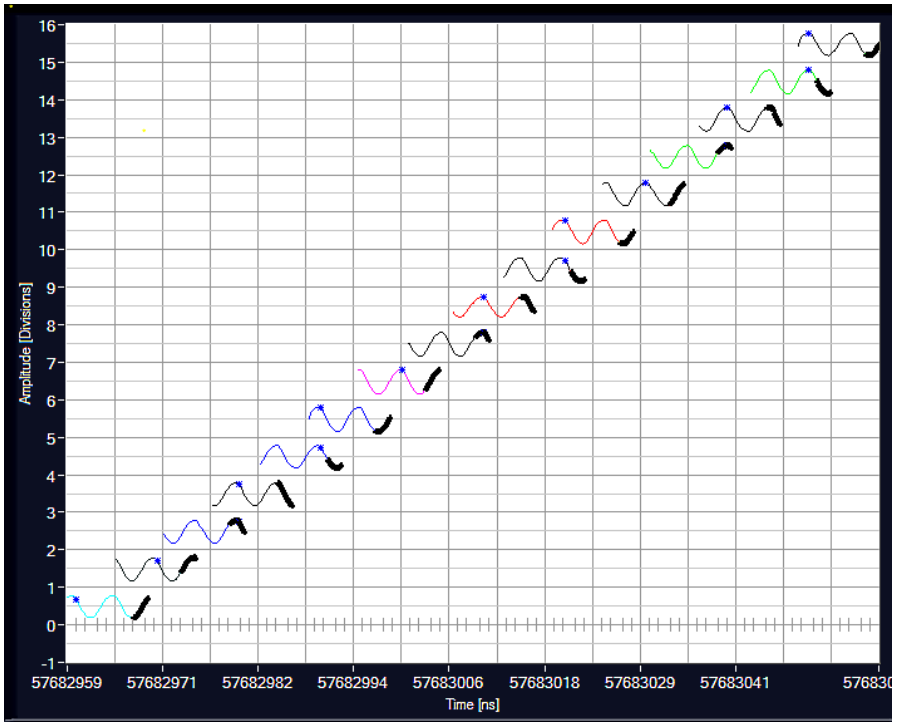
DeadTime (measured with 2 random pulses)
=> Time difference distribution

CHAIN MODE

- Goal: extend the depth of SAMPIC by **chaining channels** connected to the same source or force triggering of successive channels
- Each channel can be defined as a Master that can successively trigger N (1 to 15) other « Slave » channels.
- Tens of possible configurations
- The delay between the channels is defined by the POSTTRIG



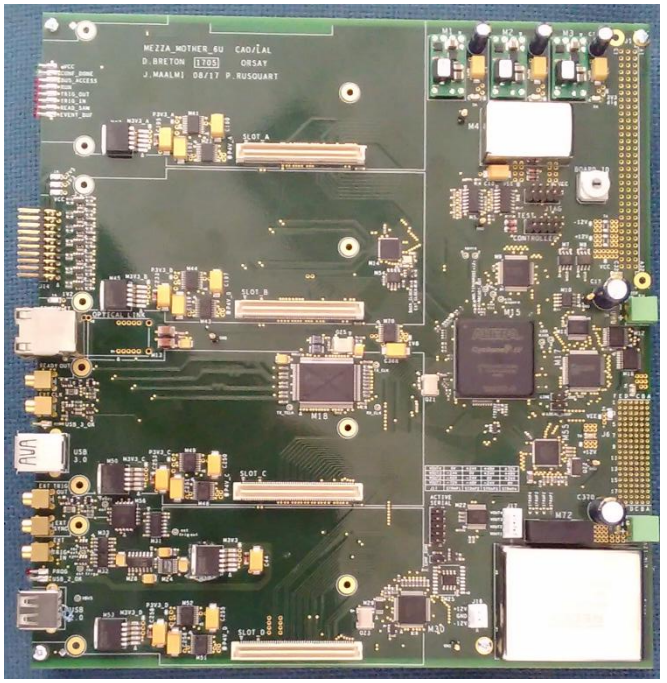
2 channels chained @1.6GSPS

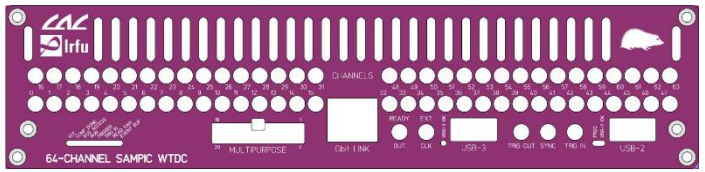


16 channels chained @6.4GSPS

BOARD & MODULE DEVELOPMENT

- A new motherboard has been designed. It can house up to 4 mezzanine boards, which permits realizing 64-channel desktop systems.
  - 2 such modules can easily be synchronized => 128 channels
  - It is also compatible with the WaveCatcher mini-crate which can house up to 4 such boards (+ a controller board), which permits realizing 256-channel compact systems.

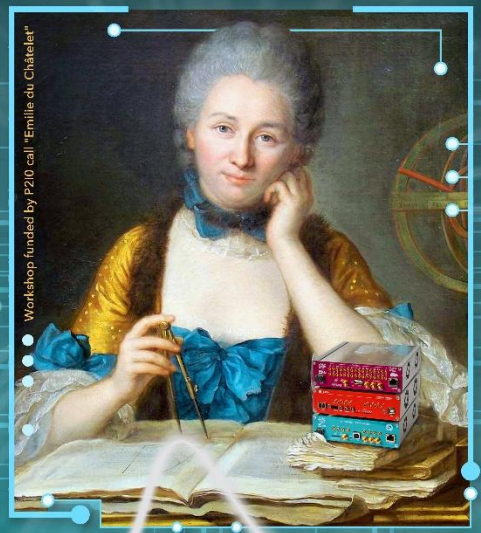




WAVECATCHER AND SAMPIC USERS' INTERNATIONAL WORKSHOP AT LAL

WaveCatcher and SAMPIC
International Workshop

February 7-8, 2018, LAL Orsay, France



Organising committee:

Dominique Breton *LAL*
Éric Delagnes *IRFU/SEDI*
Bernard Genolini *IPNO*
Jihane Maalmi *LAL*
Jean-Pierre Meyer *IRFU/SPP*
Viatcheslav Sharyy *IRFU/SPP*

Local Organisation:

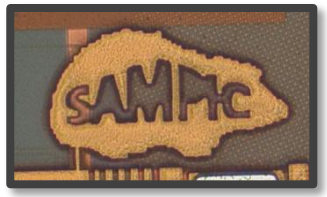
Valérie Brouillard *LAL*
Jihane Maalmi *LAL*

Call for contributions (Oral or Poster) before January, 10th, 2018 contact : maalmi@lal.in2p3.fr

Registration: http://wpsist.lal.in2p3.fr/wasiw2018/

Partner:
CAEN
Tools for Discovery

CONCLUSION



- SAMPIC is a very versatile circuit.
  - It is a full System On Chip (SOC)
    - Analog or digital input, digital output
    - All the DACs and calibration generators are integrated
    - It just requires power, clock, and a simple interface with an FPGA
    - Power consumption is as small as ~10 mW/channel
  - It samples the signal at very high rate and digitizes it.
  - All the channels can be fully independent but the TOT filter and the internal central trigger permit a smart signal noise rejection.
  - Raw counting rate can thus go >> 100 kHz/ch.
  - It can be used for a highly integrated tiny module (cm^3) as well as for large scale detectors (nuclear or high energy physics, TOF-PETs, …).
- We had only ~5 days to perform the measurements presented today
  - A lot of work remains on the chip characterization: self-calibrations, bandwidth, readout speed, time resolution between different chips, …
- Firmware and software developments are also ongoing in order to be able to deliver the new boards and modules very soon …

SAMPIC: PERFORMANCE SUMMARY

		Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption (max)	180 (1.8V supply)	mW
Discriminator noise	2	mV rms
SCA depth	64	Cells
Sampling speed	0.8 to 8.5 (10.2 for 8 channels only)	GSPS
Bandwidth	> 1	GHz
Range (unipolar)	~ 1	V
ADC resolution	7 to 11 (trade-off time/resolution)	bits
SCA noise	< 1	mV rms
Dynamic range	> 10	bits rms
Conversion time	0.1 (7 bits) to 1.6 (11 bits)	µs
Readout time / ch @ 2 Gbit/s (full waveform)	< 450	ns
Single Pulse Time precision before correction (4.2 to 8.5 GS/s)	< 15	ps rms
Single Pulse Time precision after time INL correction (4.2 to 8.5 GS/s)	< 3.5	ps rms

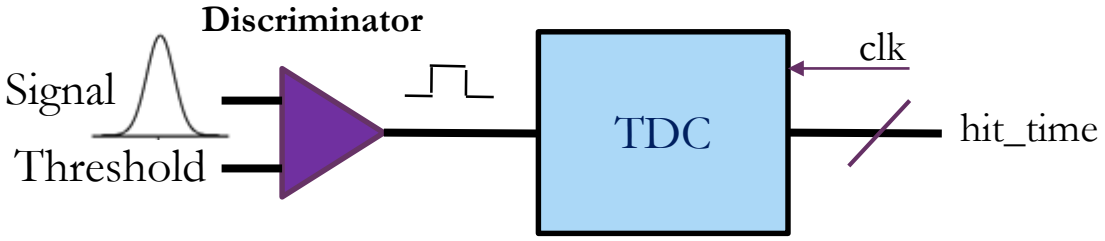
BACKUP SLIDES

- Introduction to TDC and Waveform Digitizers (5 slides)
- Zoom on the 3-switch memory cell
- Crosstalk measurement
- ADC with Auto-Conversion
- Readout philosophy
- A few slides about Time Calibration: how to reach the ps level (4 slides)
- More time measurement results (5 slides)
- TOT linearity
- NIM paper

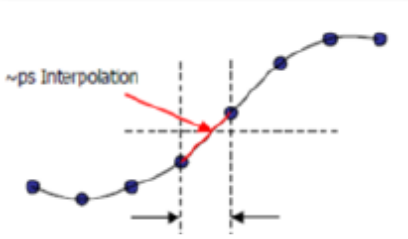
INTRODUCTION

- In the fall of 2008, the idea that time measurement at the picosecond level was going to become a main goal in the coming decades was rising in the community.
  - This was implying developments for both detectors and electronics
  - Here we will focus on electronics …

- There were (are) two main ways to measure the arrival time of a signal:
  - Using a discriminator and a Time to Digital Converter (TDC)



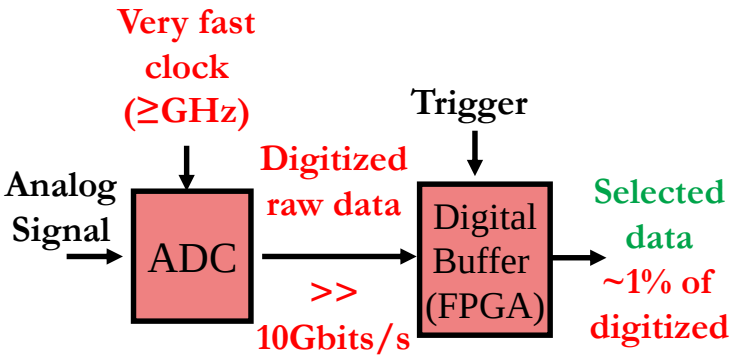
  - Digitizing the signal with a sufficient sampling frequency to be able to extract the time from the digitized waveform



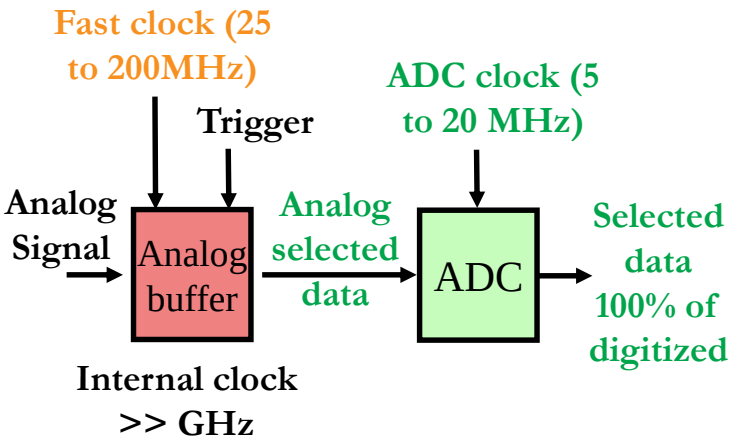
  - This became possible with the progress of digitizers, based on Analog to Digital Converters (ADCs) or Fast Analog Memories
  - Simulations showed that sampling above a few GS/s together with a good SNR (~10bits) was leading way to the ps level

ANALOG MEMORIES VS ADCs

- In terms of digitizers, high-end oscilloscopes are the costly grail (>25k€/ch) but with only 4 channels …
- They are based on fast interleaved ADCs
- High precision measurement implies high sampling rate (>> GS/s) => huge amount of data (10 to 100 Gbits/s per channel), high power
- Digitizers based on analog memories (SAMLONG, DRS4, TARGET, BLAB…) are a nice solution because:
  - they can sample the signal as fast as the ADCs
  - they digitize only useful data at lower speed => smaller cost and power
  - TDC is "built-in" (position in the memory gives the time)
  - but their readout dead-time (~2 to a few 100's µs) limits the rates and all channels are usually triggered together (oscilloscope like)
- Analog memories are a widely used solution for high precision time measurements at high scale



ADC-based digitizer



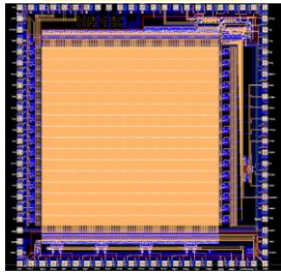
Analog_memory-based digitizer

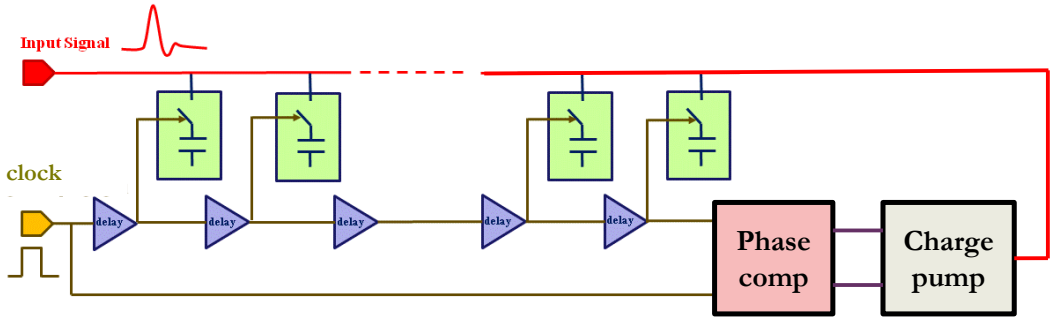
OUR FORMER DEVELOPMENTS OF ANALOG MEMORIES FOR WAVEFORM DIGITIZING

• We started designing analog memories in 1992 with the first prototype of the Switched Capacitor Array (SCA) for the ATLAS LARG calorimeter. **80,000 HAMAC chips produced** in 2002 and mounted on the 1628 boards which measured the Higgs energy. They are still on duty on the LHC for a while …

• Since 2002, many new generations of fast samplers have been designed (ARS, MATACQ, SAM/SAMLONG): **more than 50,000 chips in operation**.

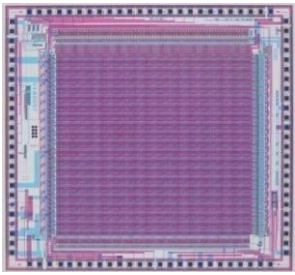
HAMAC
1998-2002





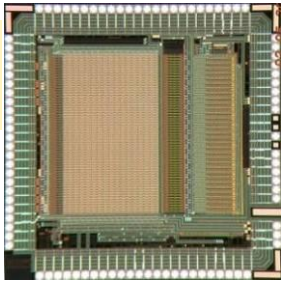
Principle of Sampling with a Delay Line Loop

MATACQ
2000-2003

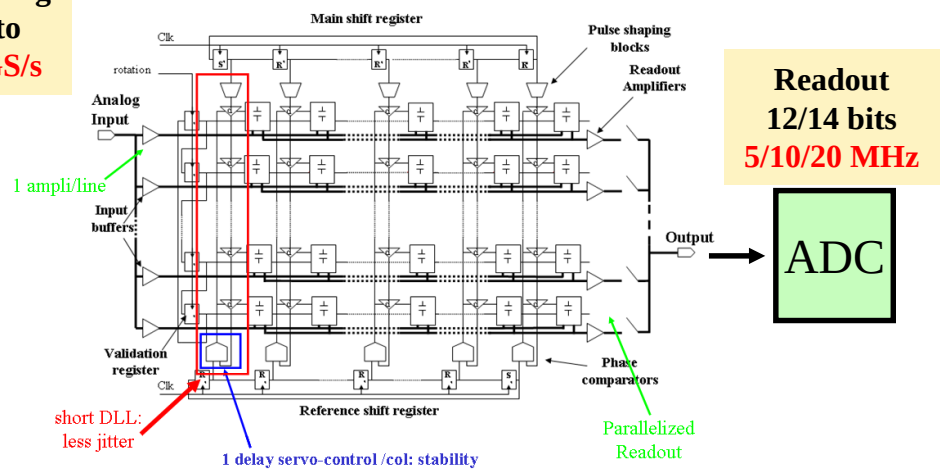


Sampling up to 3.2 GS/s

SAM
2005



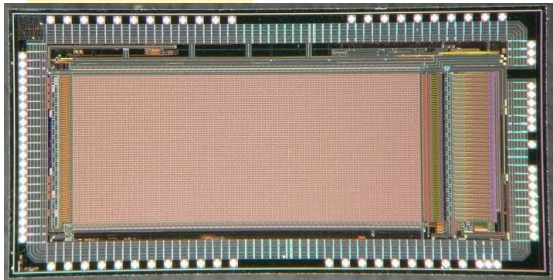
Principle of the Sampling Matrix



Readout 12/14 bits 5/10/20 MHz

ADC

SAMLONG
2010-2012



© Patented in 2001

A FEW COMMENTS ABOUT TDCs

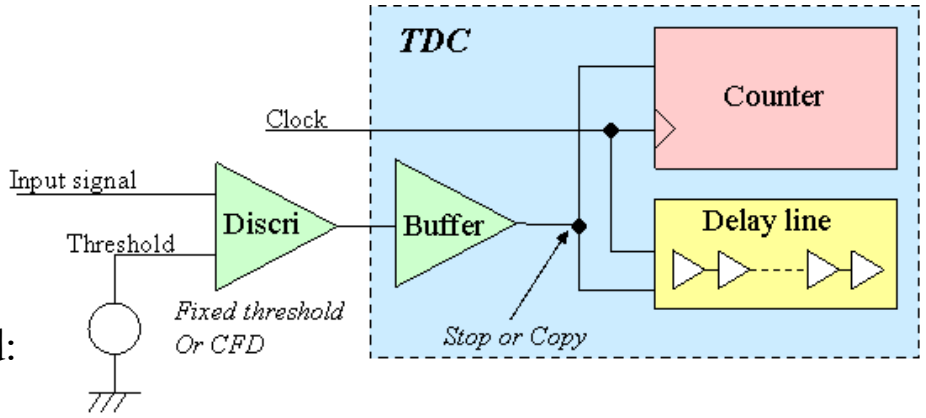
TDCs can be integrated inside ASICs or FPGAs.

- **TDCs** are specifically used for **time measurement**
  - Input counting rate can be very high (>> 40 MHz/ch)
  - Information is concentrated => autonomous channels, reduced dataflow, good for large scale
  - But they do not provide information on waveform, except **TOT**, and they work on **digital signals**

Most **fast TDCs** are using**:**

- **digital counters => coarse timestamp**
- **servo-controlled or continuously-calibrated Delay Line Loops (DLLs) => fine timestamp**

Their resolution is fixed by the DLL step
(or by an interpolation between DLL steps)



In the timing chain, a **discriminator** is required:

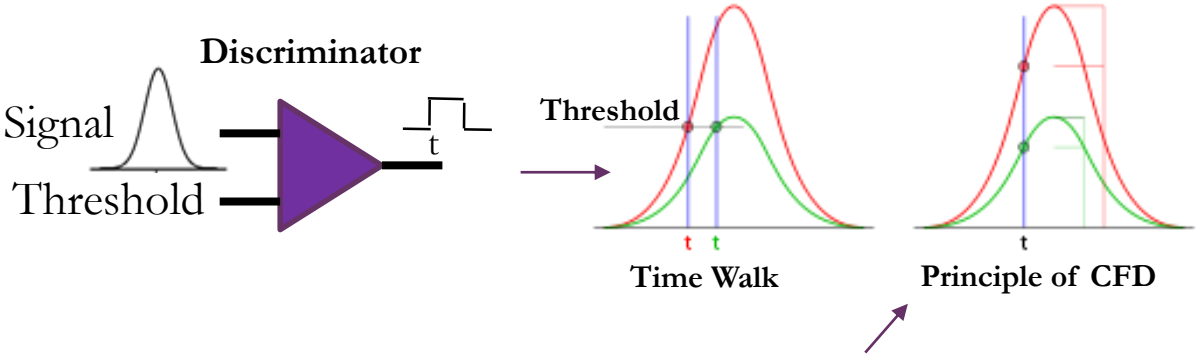
- **critical and often high power**
- Adds **additional jitter** and **residues of time walk** (even with TOT)

Like for ADCs, output dataflow can be a problem at high rates (> Gbit/s /ch)!

FOCUSSING ON DISCRIMINATORS

A discriminator translates an analog signal into a digital pulse.

When sending a signal to a discriminator, the time instant "t" of the output level toggle will depend on the amplitude of the signal => "Time Walk" Effect

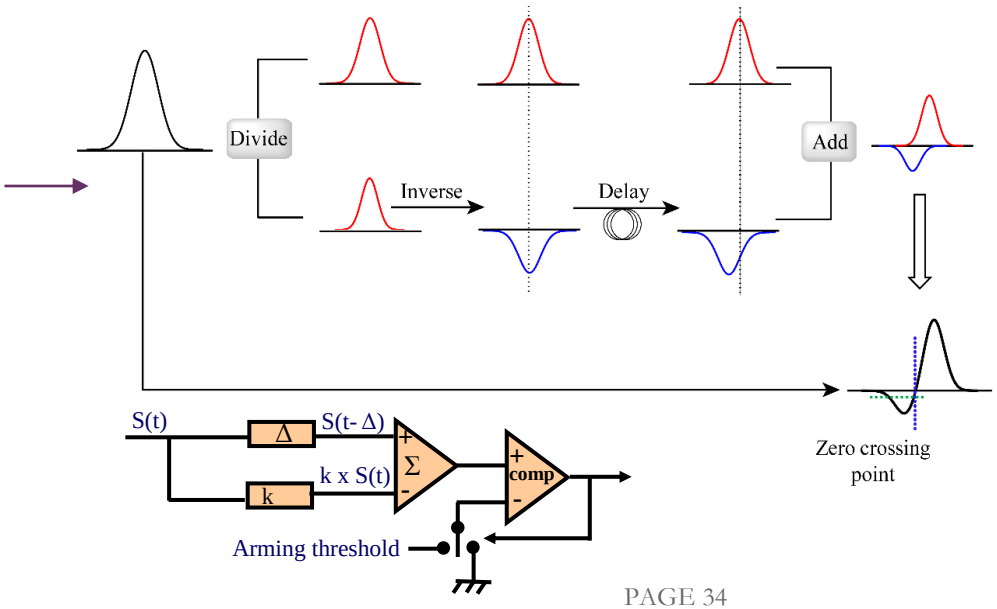


To avoid this effect, one has to use a Constant Fraction Discriminator (CFD)

- But this implies that you need to know the value of the peak to apply the threshold !
- Ok for a firmware or software when the signal has been digitized but not in a TDC …

How to make a CFD in an analog way in front of a TDC:

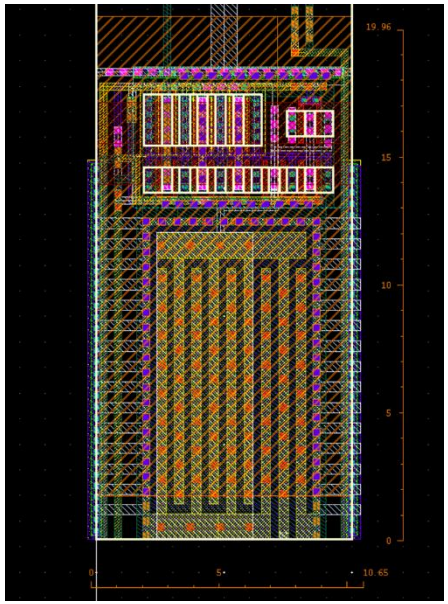
- but never perfect (there is always a residue of time walk)
- hard to integrate in an ASIC because of the delay line (needs inductances) => other options are used but they degrade the performance



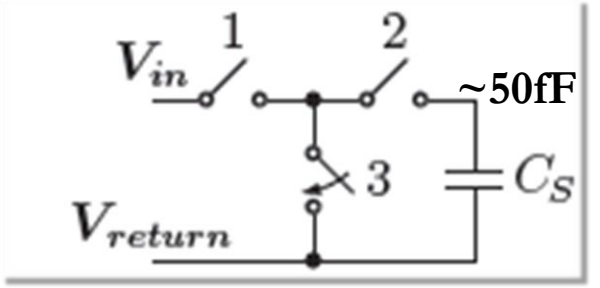
The “3-switch” memory cell

- **Design constraints:**
  - Settling time at 10^{-3} within 800ps (8 cells @10GS/s)
  - Bandwidth > 1.5 GHz
  - Non linearity < 1%
  - Dynamic range ~ 1V

Layout
size : 20x10 µm²



➡ **3 switch memory cell developed for reducing the leakage currents and the ghost effect (residue of event N-1 on event N)**



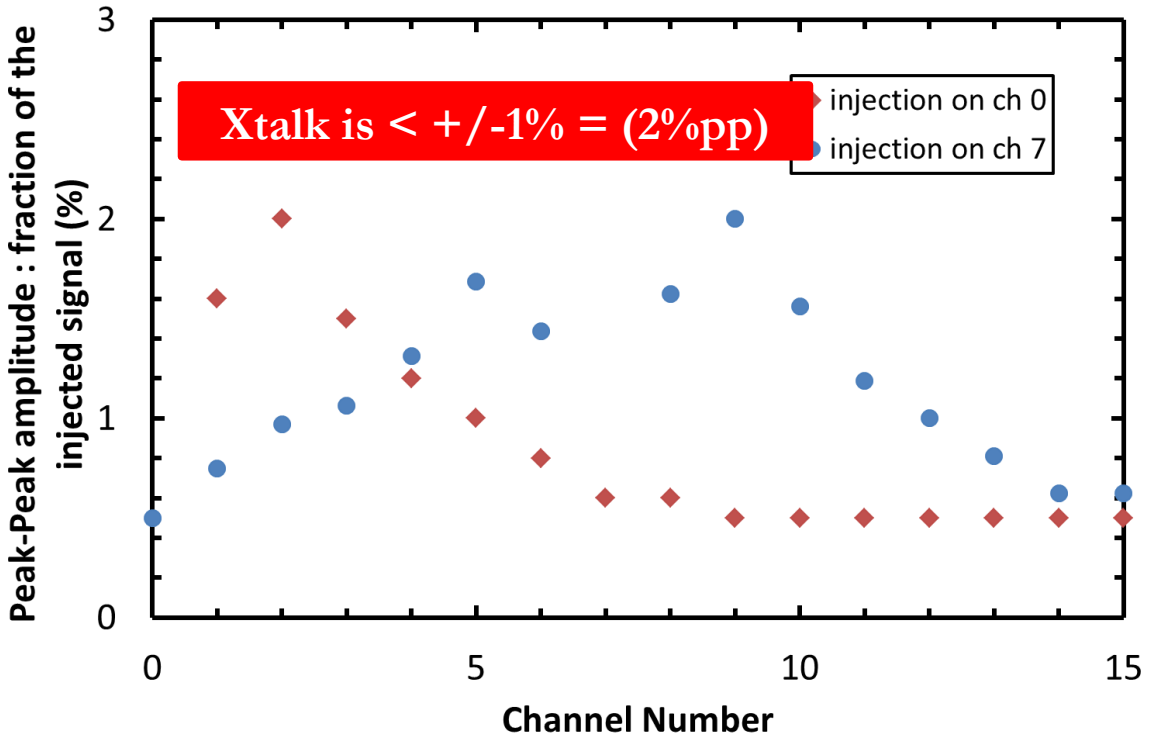
3-switch memory cell

Charge injections when opening switch 2
=> major source for Integral Non Linearity
=> size of switch 2: tradeoff between
RDSon / Bandwidth (→ wide W_{MOS})
Injected charge / INL (→ narrow W_{MOS})

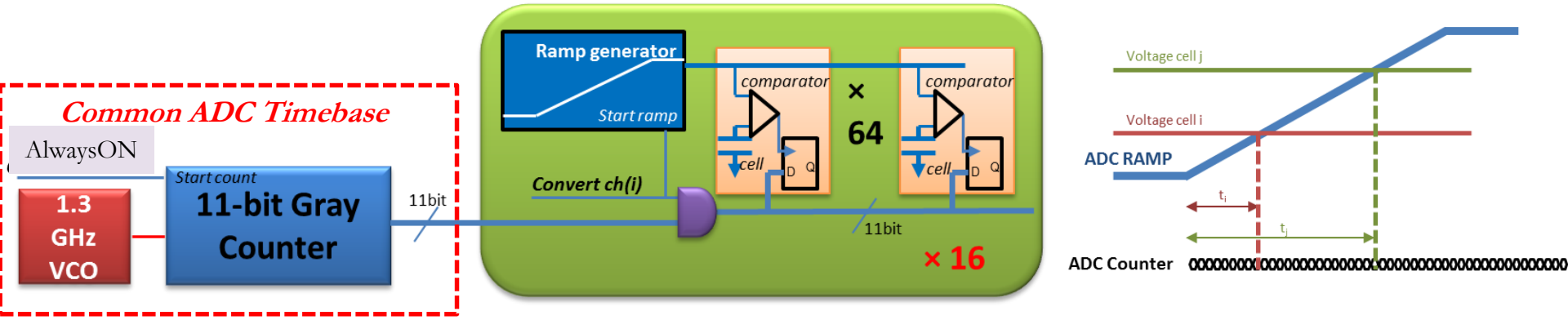
Simulation results: INL ~0,2% max for Vin from 50mV to 1V

SAMPIC_V0: XTALK MEASUREMENT

- 800mV, 1ns FWHM, 300ps risetime and falltime injected on **channel 7 (blue)**
- Signal measured on the other channels
- Xtalk = derivative and decrease as the distance to the injection channel
- Xtalk signal is bipolar with ~ equal positive and negative lobe
- Similar plot, but shifted if injection in another channel **(red)**



WILKINSON ADC WITH AUTO-CONVERSION MODE



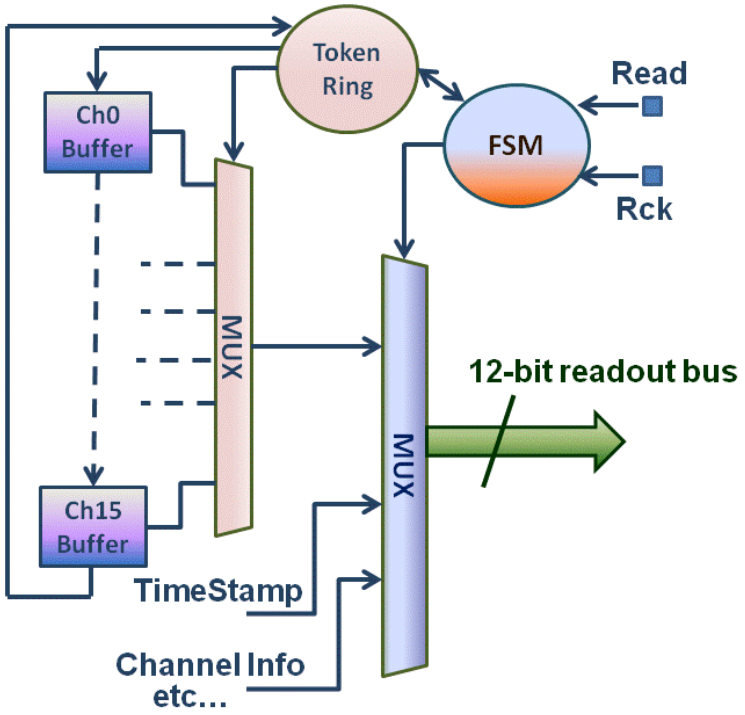
- **When triggered, each channel launches its auto-conversion.**
  - When ramp starts, the value of the continuously running counter is sampled in a dedicated channel register
  - When the ramp crosses the cell voltage => the current value of the counter is stored in the cell register (ramp offset).
  - **As soon as all discriminators of the channel have fired, Analog to Digital conversion of the channel is over => optimization of dead time**
  - During readout, the ramp offset is read before the channel waveform samples.

In "auto-conversion" mode , the ramp offset will be subtracted from the value of the waveform samples.

READOUT PHILOSOPHY

- Readout driven by **Read** and **Rck** signals => **controlled by FPGA**
- Data is read **channel by channel** as soon it is available
- Rotating **priority mechanism** to avoid reading always the same channel at high rate
- **Optional Region Of Interest readout** to reduce the dead time (**nb of cells read can be chosen dynamically**)
- Readout of converted data through a 12-bit parallel LVDS bus including:
  - Channel Identifier, Timestamps, Trigger Cell Index
  - The cells (all or a selected set) of a given channel sent sequentially
  - Standard readout at 2 Gbits/s

  => **Rate > 2 Mevts/s (full waveform)**



- **Channel is not in deadtime during readout, only during conversion (data register is really a buffer stage)**

CALIBRATION PHILOSOPHY

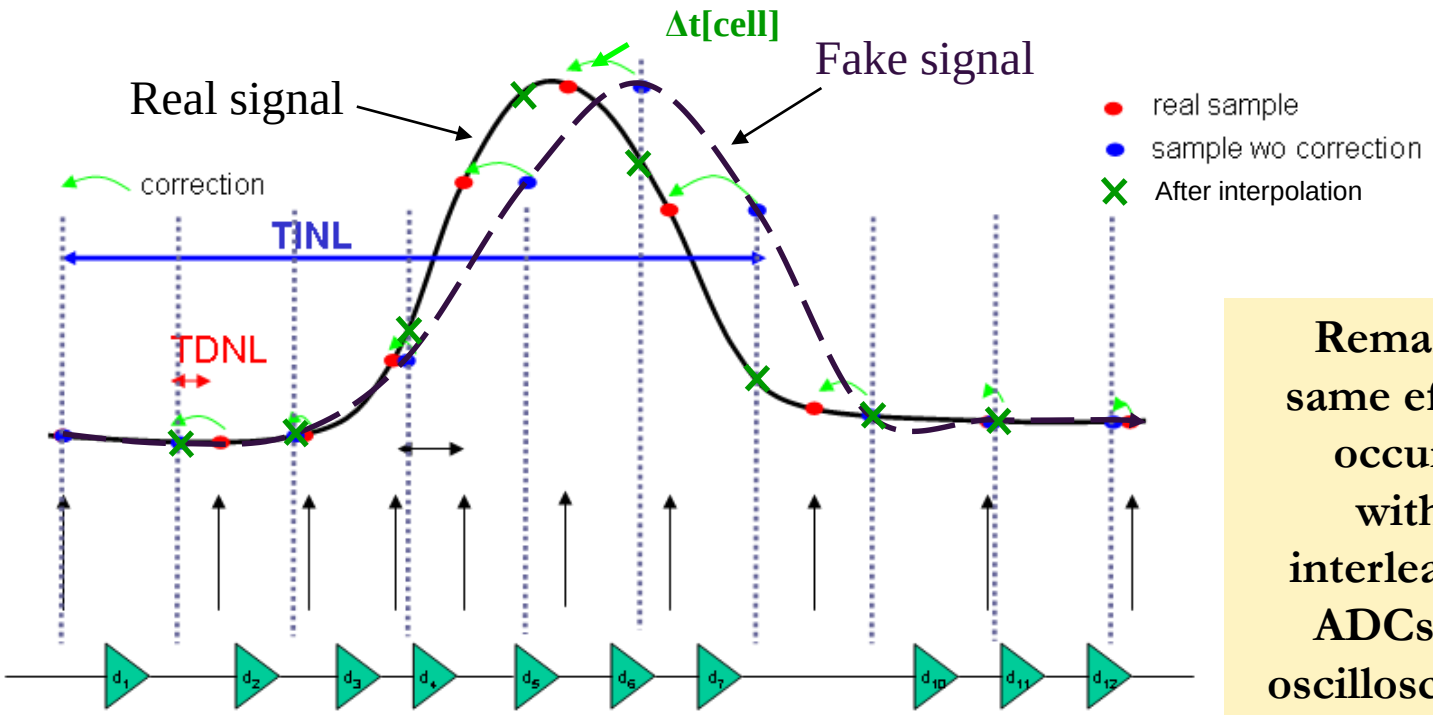
- SCAs-based chips exhibit reproducible non-idealities which can be easily corrected after calibration:
  - The goal is to find the set with the **best performance/complexity ratio**.
  - But also to find the right set for the **highest level of performance**.
- SAMPIC actually offers very good performance with only two types of simple calibrations :
  - **Amplitude: cell pedestal and gain** (**linear** or **parabolic** fit) => DC ramp
  - **Time: INL** (one offset per cell) => use of a **simple sinewave** (see backup)
  - This leads to a limited volume of standard calibration data (**4** to **6** Bytes/cell/sampling frequency => **5** to **8** kBytes/chip/sampling frequency) => can be stored in the on-board EEPROM (1Mbit).
- These simple corrections could even be applied **in the FPGA**.
- Highest level calibrations permit debugging the chip and pushing the performance to its limit (still unknown).

TIMING NON-LINEARITIES

- Dispersion of single delays => **time DNL**
- **Cumulative effect** => **time INL**. Gets worse with delay line length.
- **Systematic & fixed effect** => non equidistant samples => Time Base Distortion

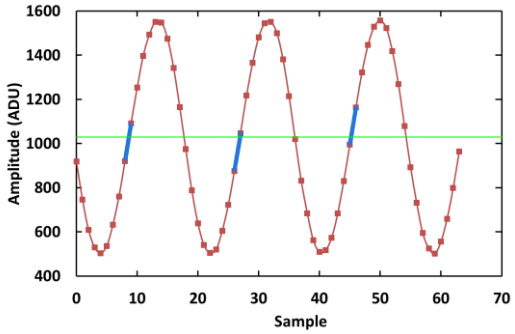
If we can measure it => we can correct it !

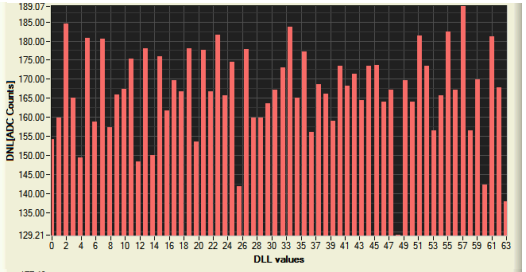
But calibration and even more correction have to remain "simple".

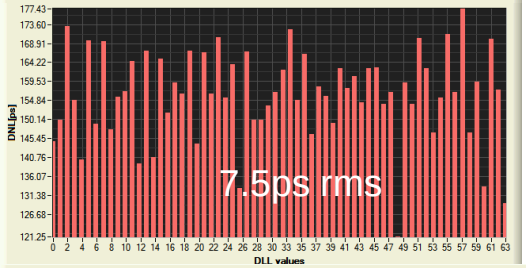


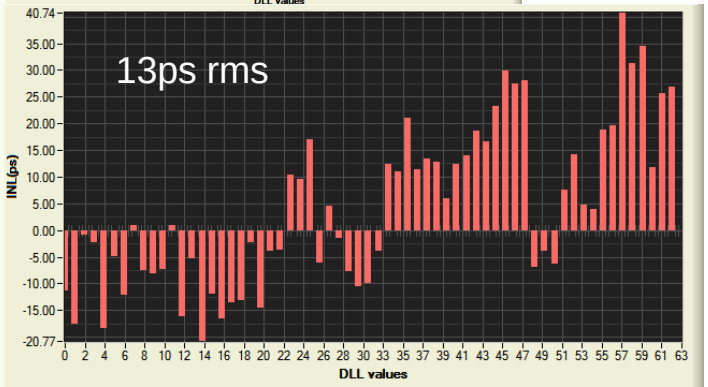
Remark: same effect occurs with interleaved ADCs in oscilloscopes

TIME INL CALIBRATION AND CORRECTION









Method we introduced in 2009 and used since for our analog memories, assuming that a sinewave is nearly linear in its zero crossing region: much more precise than statistical distribution

- Search of zero-crossing segments of a free running asynchronous sine wave

  => length[position]
- Calculate the average amplitude for zero-crossing segment for each cell.
- Renormalize (divide by average amplitude for all the cells and multiply by the clock period/number of DLL steps)

  => time duration for each step = "time DNL"
- Integrate this plot:

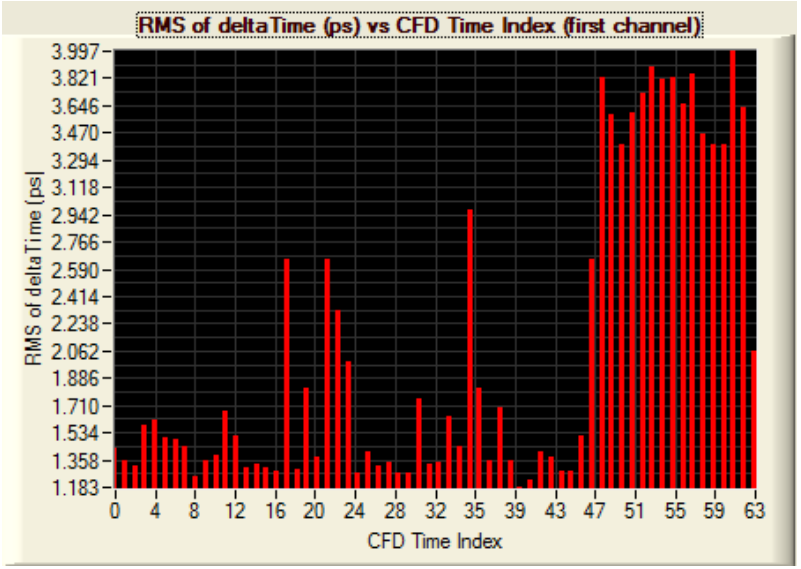
  ⇒ Fixed Pattern Jitter = correction to apply to the time of each sample = "time INL"

Time INL correction:

- **Simple addition** on T_{sample}
- Also permits the calculation of real equidistant samples by interpolation or digital filtering.

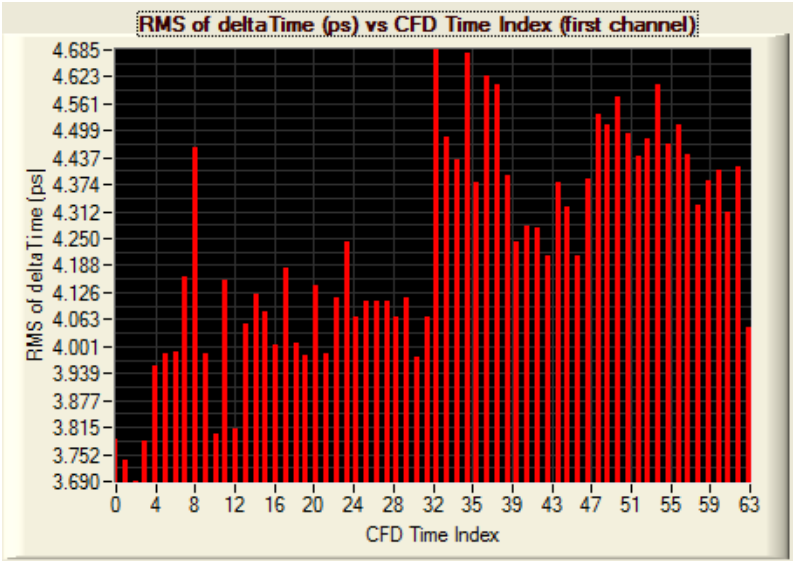
TRICKS FOR UNDERSTANDING RESOLUTION

- This is how we measure the contributions to the resolution: we run at 6.4 GS/s, send two 500 mV pulses separated by 2.5 ns to two channels:
  1. of the same mezzanine
  2. of two different mezzanines



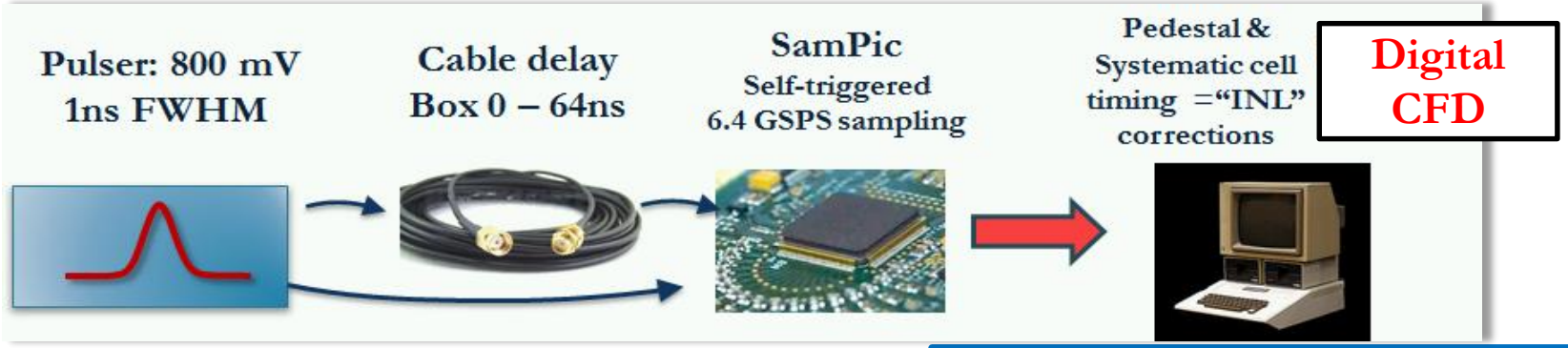
Same chip

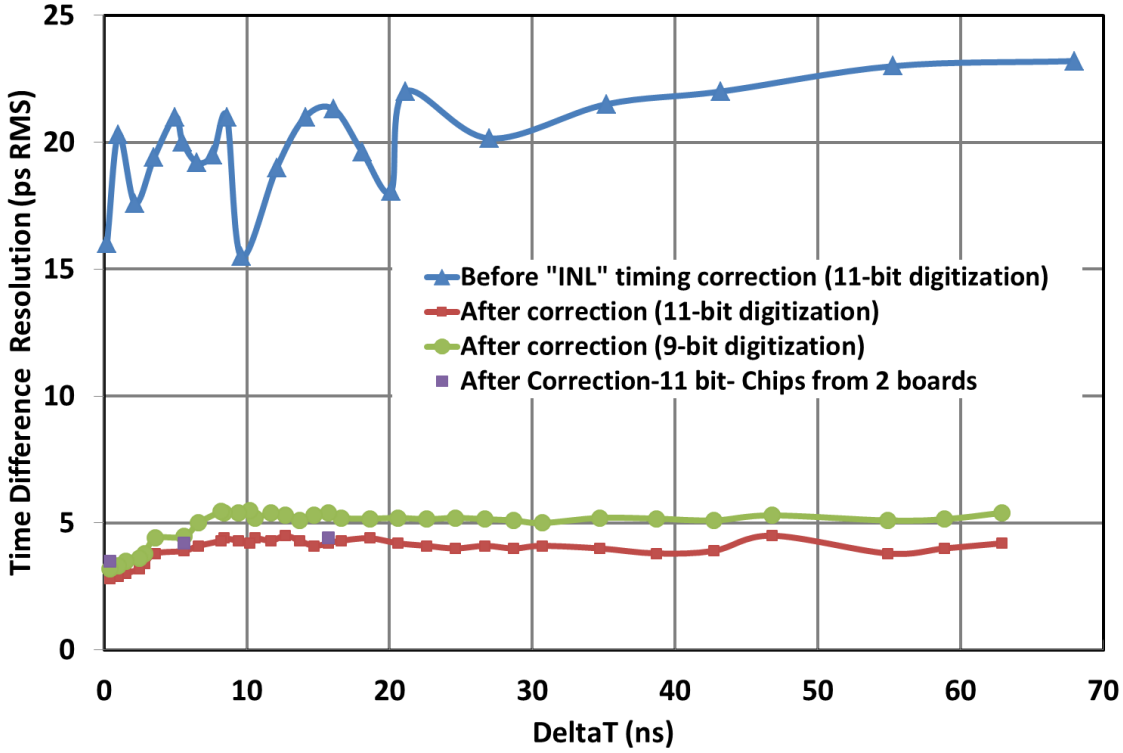
- From this we can extract that **the jitter contribution is:**
- **~ 1.5 ps rms from the DLL**
- **~ 1.8 ps rms from the clock distribution on the motherboard**
- **~ 2.4 ps rms from the clock distribution on the mezzanine**



Different chips

ΔT RESOLUTION VS DELAY





- TDR < 25 ps RMS before time cor.
- TDR < 5 ps RMS after time cor.
- TDR is constant after ΔT=10ns
- Unchanged for 2 chips from 2 different mezzanines (same clk source but different DLLs and on-chip clock path)

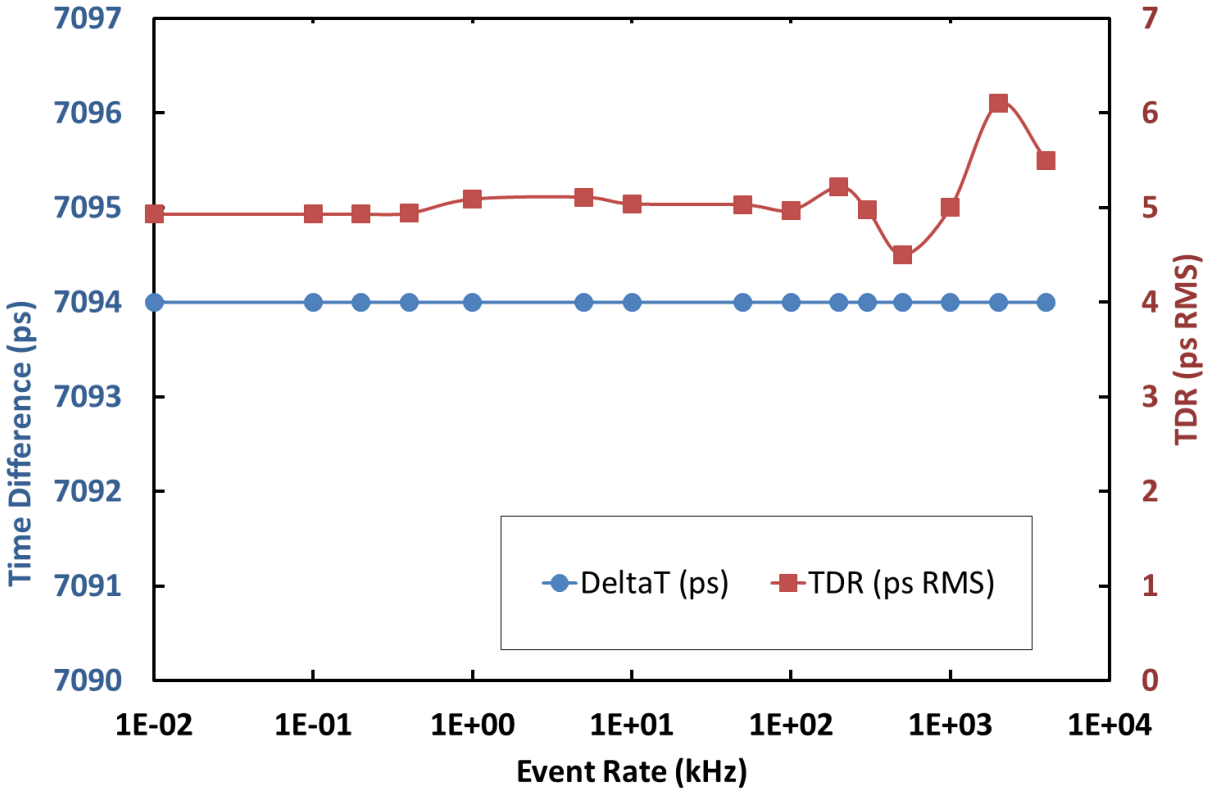
=> Channel single pulse timing resolution is < 3.5 ps RMS (5 ps/√2)

- For these large pulses TDR is worst by only 1ps RMS in 9-bit mode (digitization time divided by 4)

TIMING RESOLUTION VS RATE

1ns FWHM, 400ps risetime, 0.7V signals sent to 2 channels of SAMPIC

- 7.1ns delay by cable, 6.4 GS/s, 11-bit mode, 64 samples, both INLs corrected
- Rate is progressively increased.

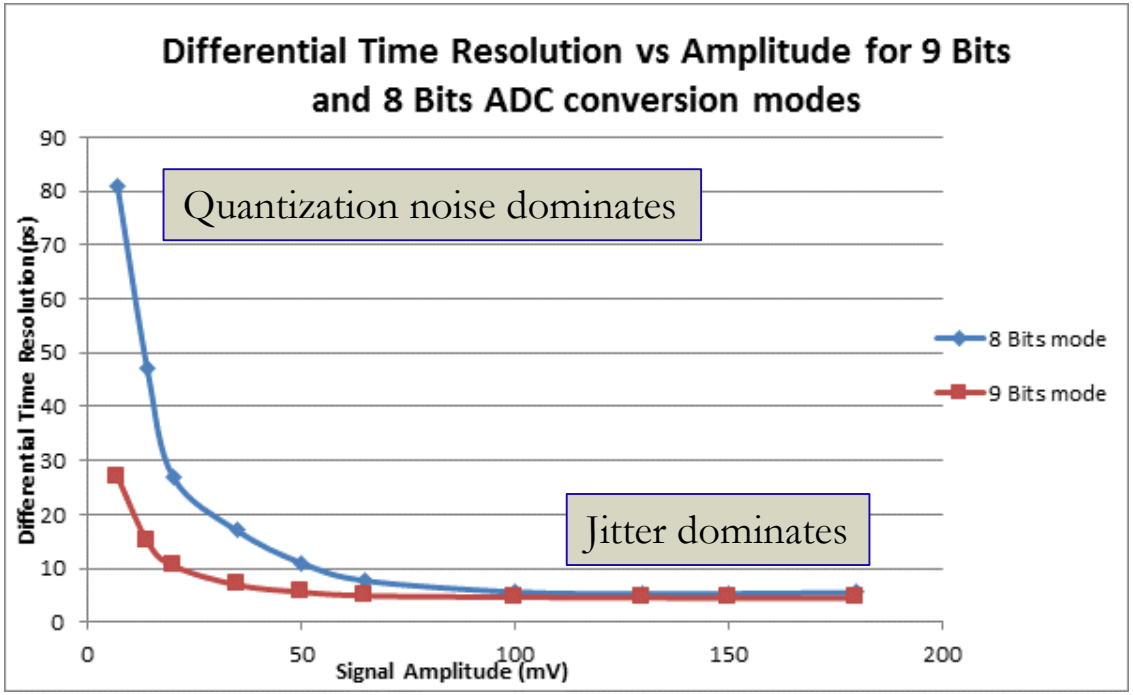


The measured delay and its resolution are stable for channel rates up to 2 MHz

TIMING RESOLUTION (DIGITAL CFD) VS ADC NUMBER OF BITS

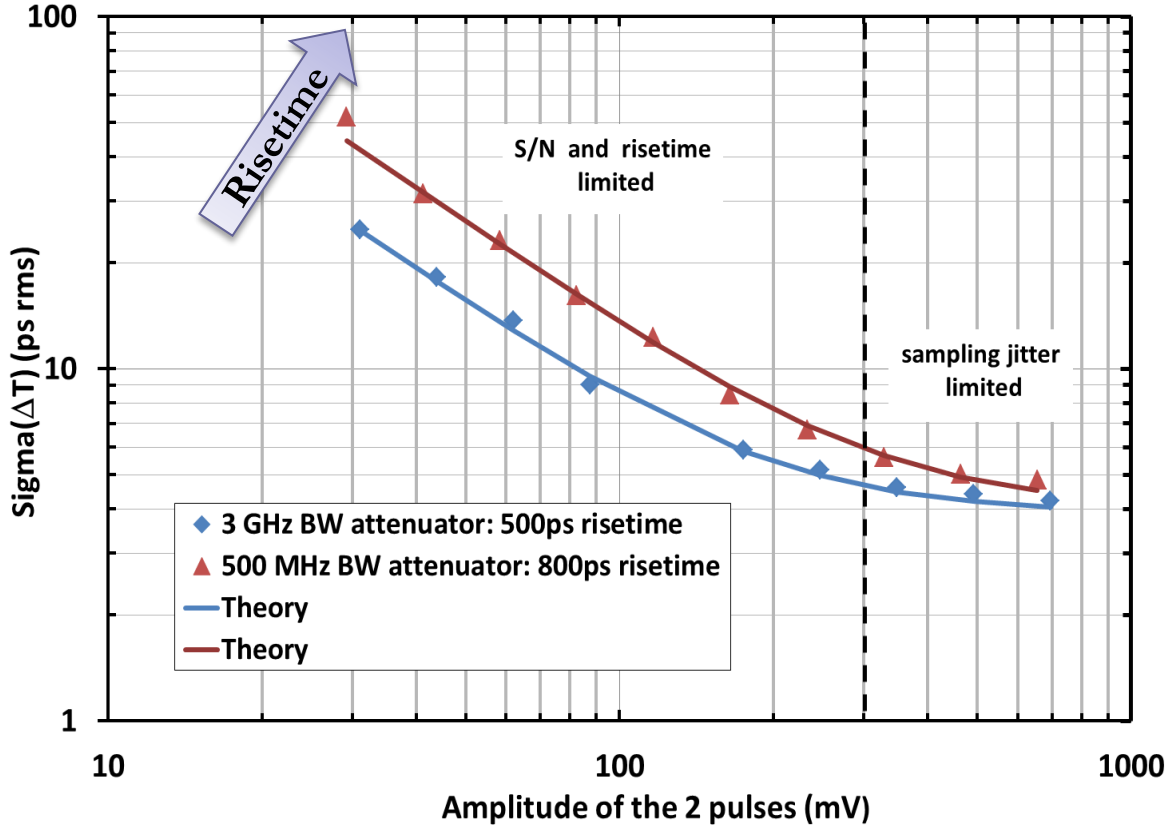
- In order to **minimize dead-time**, ADC number of bits can be reduced: factor 2 for **10 bits (800 ns), 4 for 9 bits (400 ns), 8 for 8 bits (200 ns), 16 for 7 bits (100 ns).**
- Looking at the effect of the ADC number of bits on time resolution…
- Signal amplitude is the key element in this case: **time resolution degrades for small signals since quantification noise becomes dominant**

- There is **very small loss** in performance between 11, 10 and 9-bit modes.
- Where quantization noise dominates, other methods than dCFD can be used …



No degradation on timing for pulses above 100mV for 8 bits & 50mV for 9 bits

TIMING RESOLUTION VS AMPLITUDE & RISETIME
1-NS FWHM - 15 NS DELAY, DIGITAL CFD ALGORITHM



Measurements consistent with the theoretical formula:

$$\sigma(\Delta t) = \sqrt{2} \times \sqrt{\sigma_j^2 + \alpha \times \left(\frac{\sigma_n}{Slope}\right)^2}$$

Assuming: :

* Voltage noise σ_n = 1.1 mV RMS
* Sampling jitter σ_j = 2.8 ps RMS
* $\alpha = 2/3$ (simulation of perfect CFD)

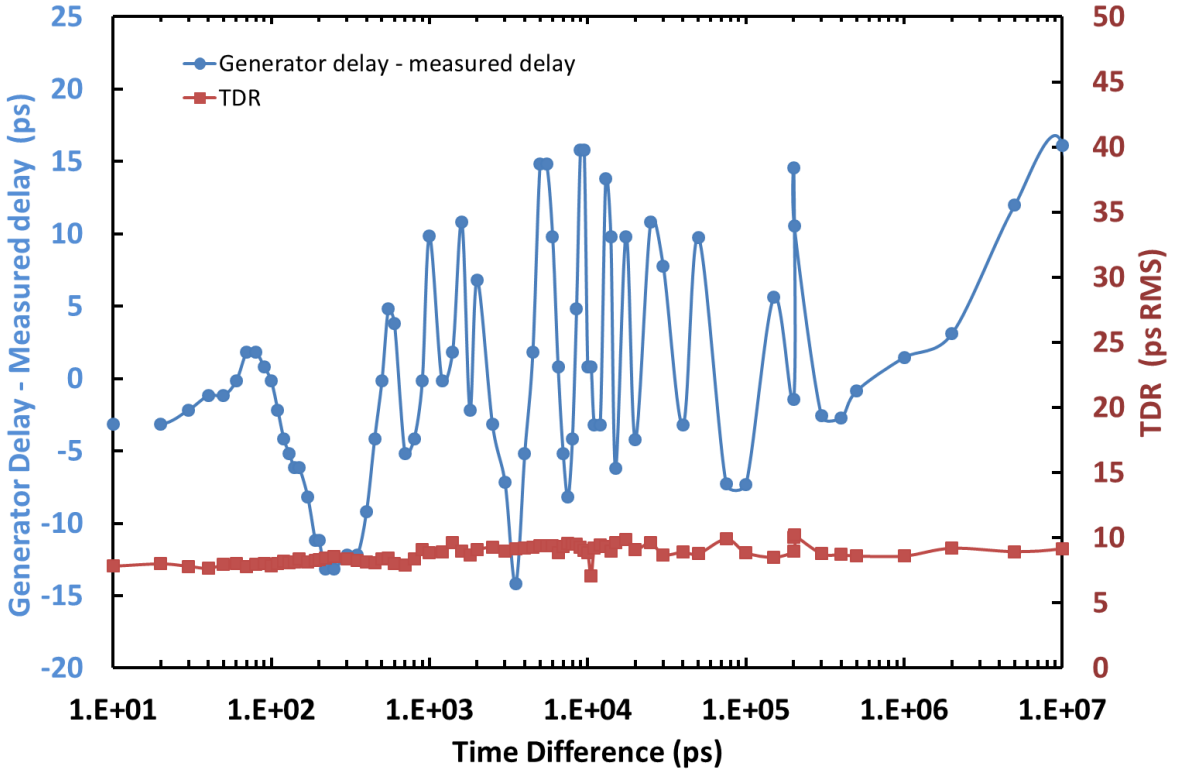
- 2 zones: sampling jitter or S/N limited zones.
- TDR < 8 ps rms for pulse amplitudes > 100mV
- TDR < 20 ps rms for pulse amplitudes > 40 mV

- Can be improved by using mores samples (if feasible and uncorrelated) since dCFD uses only 2 samples

EXPLORING LARGER DELAYS: TOWARD AN « ABSOLUTE » TIME MEASUREMENT

- Now we use 2 channels of a TEK AFG 3252 arbitrary waveform generator and program their relative delay (10-ps steps)
- Slower than the previous generator (2.5ns risetime min)
- TEK AFG 3252 is specified for an absolute precision of few 10 ps delay and a 100ps jitter

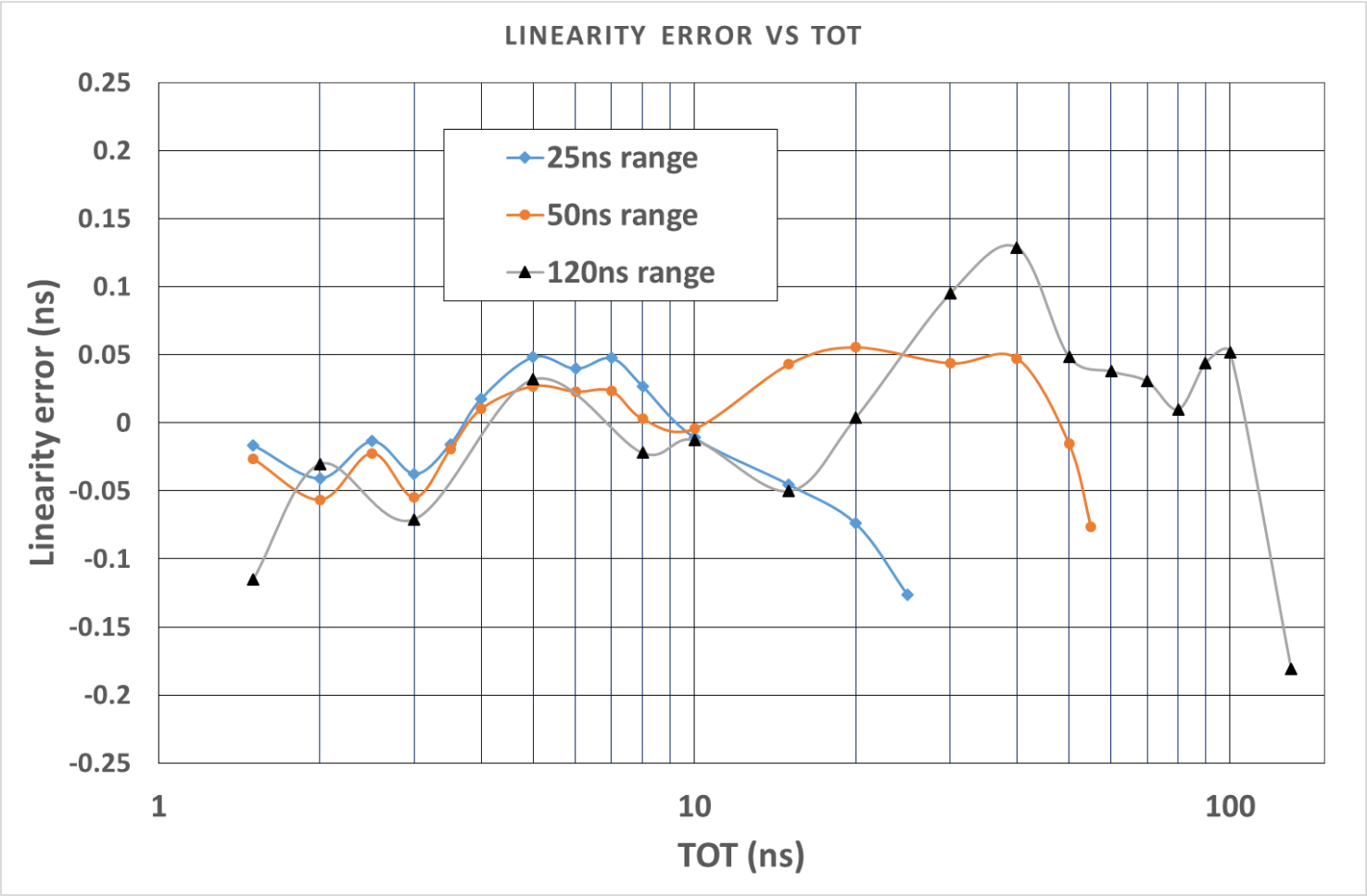
=> Measurements are clearly MUCH better



- TDR is < 10ps rms, even for delays up to 10 µs => 1-ppm RESOLUTION
- Difference between AFG programmed delay and measured value is < +/-15ps

TOT LINEARITY

- This is a preliminary plot (calibration performed is not well known).



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Measurements of timing resolution of ultra-fast silicon detectors with the SAMPIC waveform digitizer

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ABSTRACT

The SAMpler for PICosecond time (SAMPIC) chip has been designed by a collaboration including CEA/IRFU/SEDI, Saclay and CNRS/LAL/SERDI, Orsay. It benefits from both the quick response of a time to digital converter and the versatility of a waveform digitizer to perform accurate timing measurements. Thanks to the sampled signals, smart algorithms making best use of the pulse shape can be used to improve time resolution. A software framework has been developed to analyse the SAMPIC output data and extract timing information by using either a constant fraction discriminator or a fast cross-correlation algorithm. SAMPIC timing capabilities together with the software framework have been tested using pulses generated by a signal generator or by a silicon detector illuminated by a pulsed infrared laser. Under these ideal experimental conditions, the SAMPIC chip has proven to be capable of timing resolutions down to 4 ps with synthesized signals and 40 ps with silicon detector signals.

http://arxiv.org/abs/1604.02385