The ATLAS High Granularity Timing Detector for HL-LHC

L. Serin (CNRS/IN2P3/LAL)

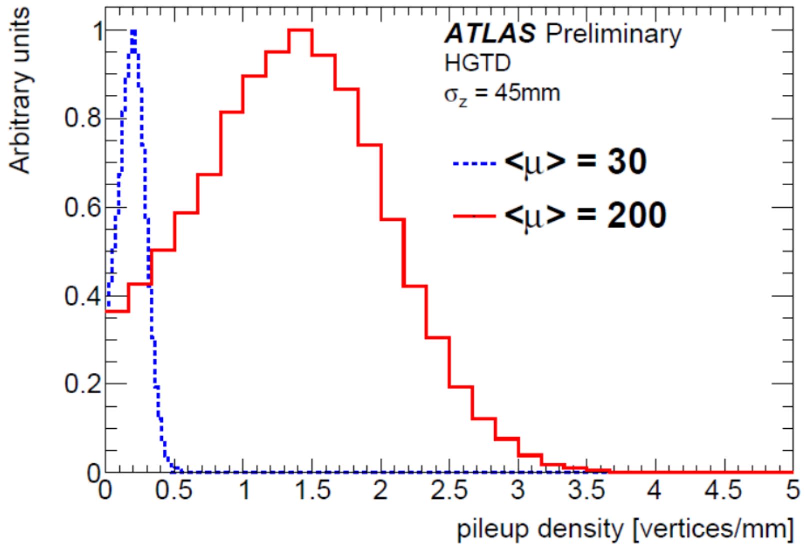
Institutes involved in HGTD : CERN, LPNHE, LAL, Omega (France), Mainz, Giessen (Germany), Casablanca (Morocco), IFAE, CNM (Spain), JSI (Slovenia), KTH (Sweden), Sinica Academia, National Tsing-Hua University (Taiwan), BNL, Stony Brook, Iowa, Ohio, SMU, SLAC, UCSC (US), JINR (Russia) +….

Most of the material is from the ATLAS HGTD TP to be made public mid June

Outline

- ATLAS phase II and Motivation for the timing detector
- Detector requirements
- Sensors R&D
- Electronics R&D
- Clock distribution and t_0 calibration
- Layout design and expected performance
- Conclusion

Motivation for precise time measurements

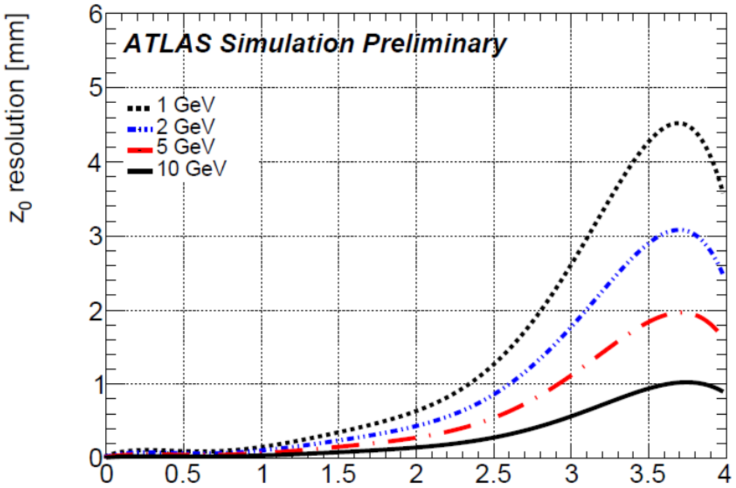


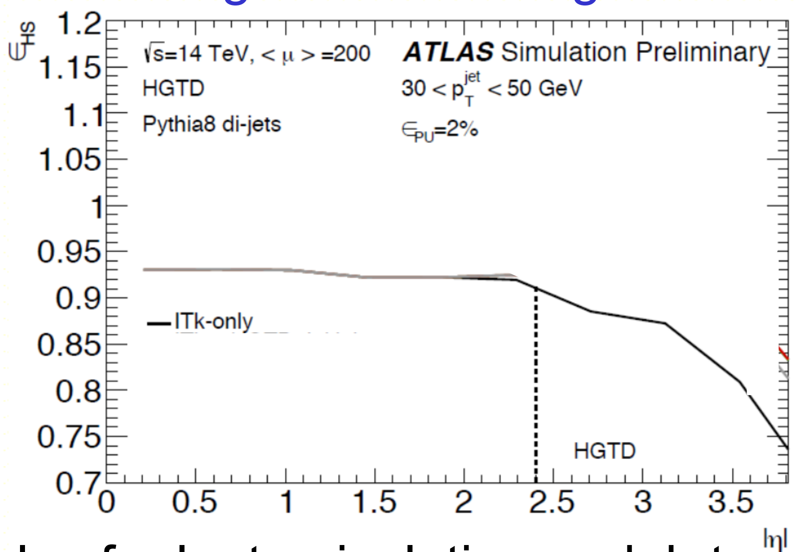
HL-LHC :

- expect <μ> = 200
- Average vertex density 1.8 vtx/mm

z_0 resolution increases with η and several vertices can be merged

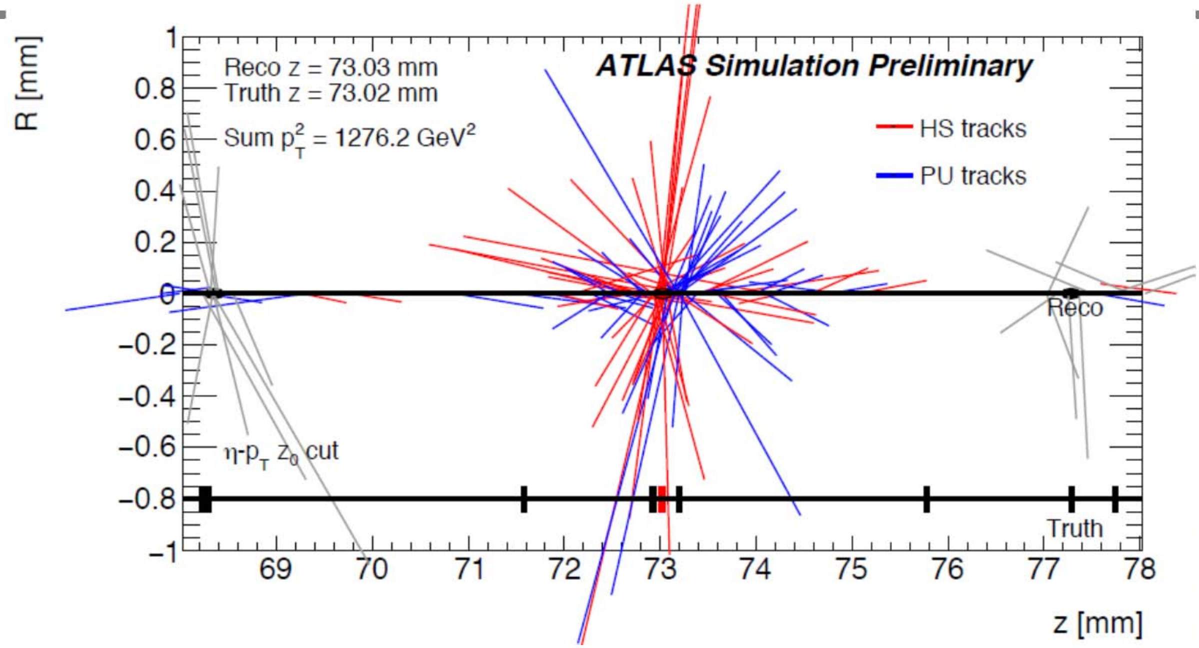
→ Degradation of performance at large η critical region for VBF signals



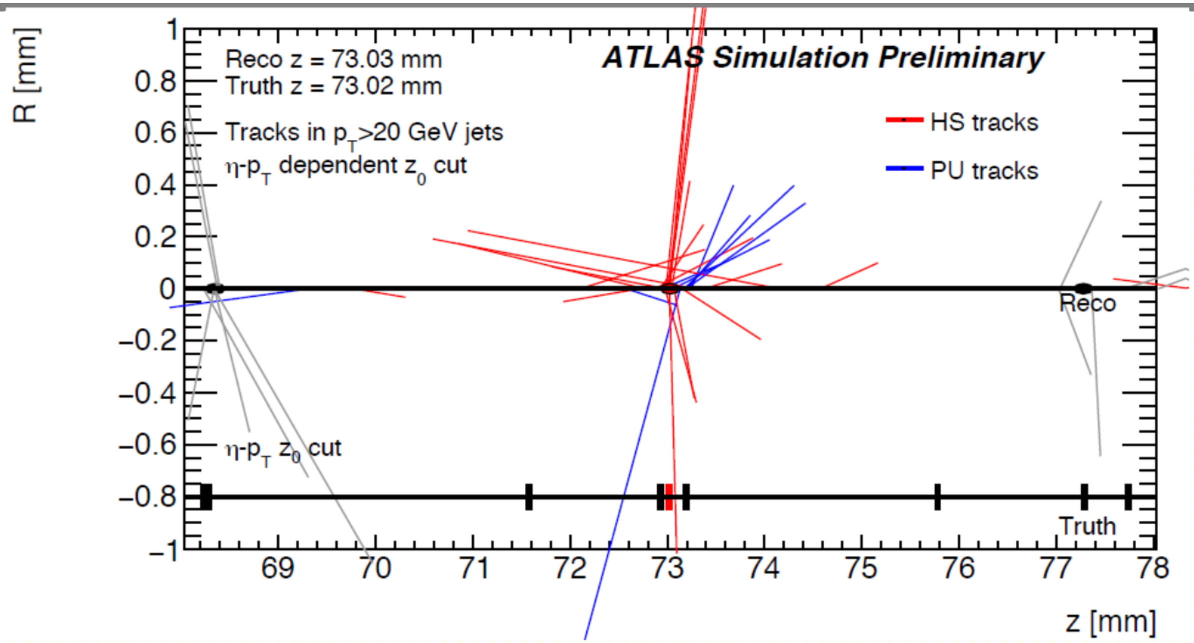


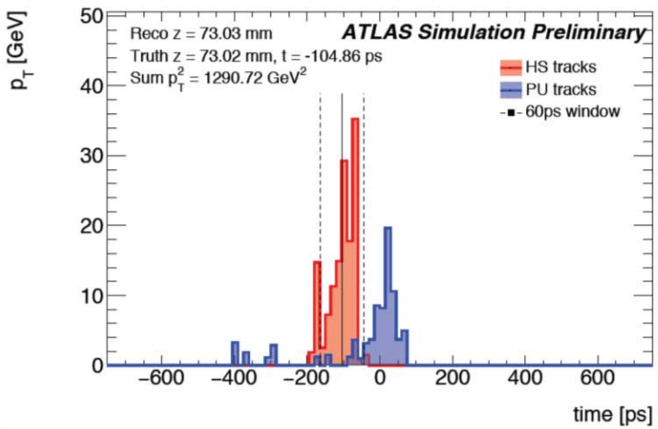
Loss also for lepton isolation and b tagging

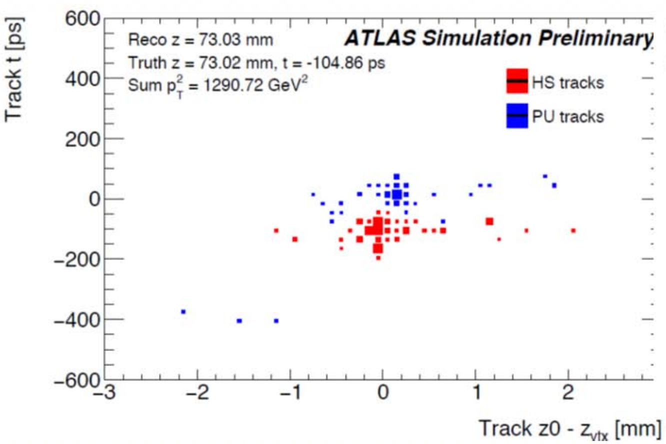
Motivation for precise time measurements (2)

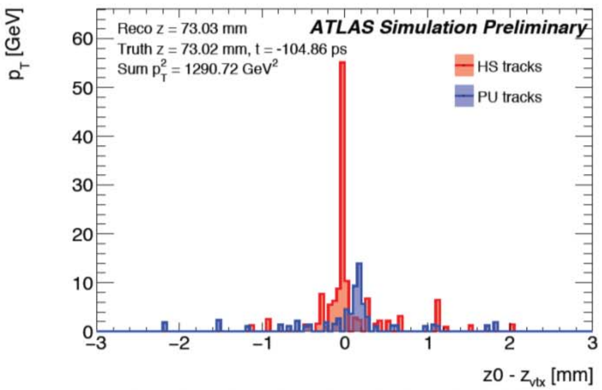


Motivation for precise time measurements (2)







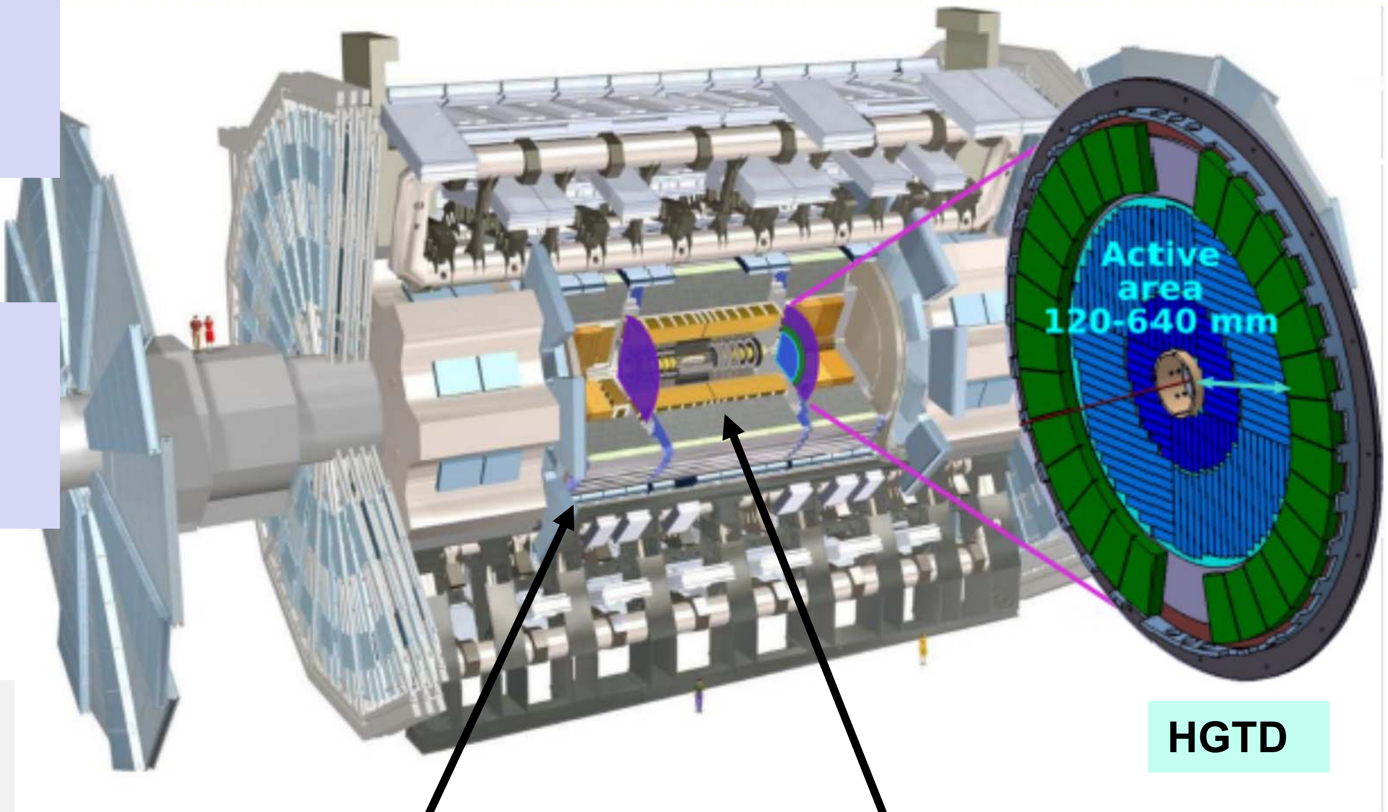


ATLAS Phase II upgrade

Upgraded Trigger and Data Acquisition System:
- L0 @1 MHz
- Improved High Level Trigger

Electronics Upgrade :
- Lar calorimeter
- Tile calorimeter
- Muon system

Options :
- High η muon tagger
- Forward detector incl. luminosity



New muon chambers in the inner barrel region

New Inner Tracking detector (all silicon tracker up to $|\eta|$ =4)

TDR Approved by LHCC

TP to be approved by LHCC

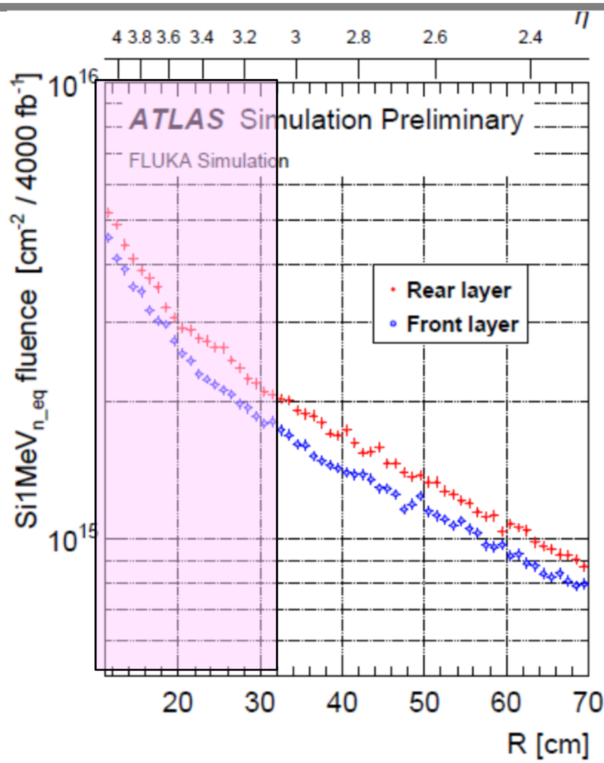
Detector Requirements

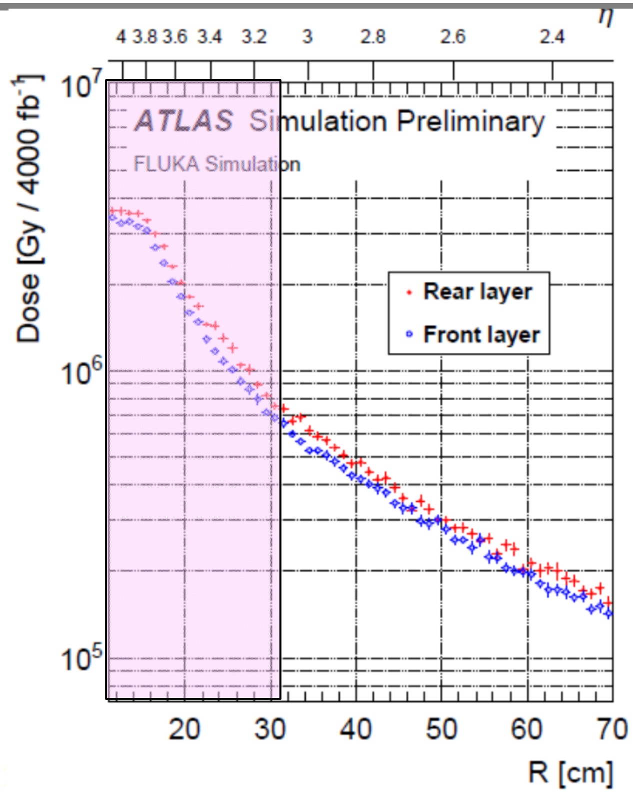
The detector is quite constrained by the space available and the harsh environment while willing to reach excellent time resolution for mip track

→ Low Gain Avalanche Diode Technology sensors

Pseudorapidity coverage	$2.4 < \|\eta\| < 4.0$
Thickness in z	75 mm (+50 mm moderator)
Position of active layers in z	3435 mm $< z <$ 3485 mm
Radial extension:	
Total	110 mm $< R <$ 1000 mm
Active area	120 mm $< R <$ 640 mm
Time resolution per track	30 ps
Number of hits per track:	
$2.4 < \|\eta\| < 3.1$	2
$3.1 < \|\eta\| < 4.0$	3
Pixel size	1.3×1.3 mm^2
Number of channels	3.54M
Active area	6.3 m^2

Radiation levels in HGTD





In addition :

- Factor 1.5 on fluence (simulation uncertainty)
- A factor 2.25 for TID (1.5 from simulation and 1.5 for dose rate effect in ASIC)

Current strategy is a replacement of the inner part (r<320 mm) at half HL-LHC running period :

max doses r < 320 mm 3.7 10^{15} neq /cm^2 and 4.1 MGy
r > 320 mm 3.0 10^{15} neq /cm^2 and 1.6 MGy

Time resolution

Total time resolution per hit :

$$\sigma^2_{\text{total}} = \sigma^2_{\text{L}} + \sigma^2_{\text{elec}} + \sigma^2_{\text{clock}}$$

Sensor R&D :
- Thickness, pad size, doping
- Radiation hardness (Ga, C spray..)

Electronics R&D :
- Dedicated ASIC
- Jitter & time walk
- Radiation hardness
- Power dissipation

Clock distribution
(CERN working group)
t0 calibration

$$\sigma_{\text{Jitter}} = \frac{N}{(dV/dt)} \simeq \frac{t_{\text{rise}}}{(S/N)}$$

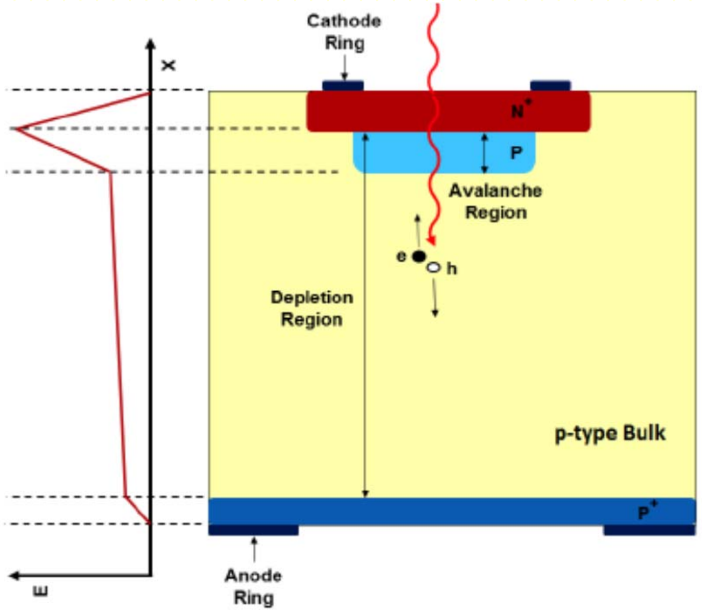
Total time resolution per track $\sigma(\text{track}) = \sigma\,(\text{hit}) / \sqrt{N_{\text{hits}}}$ goal < 30 ps

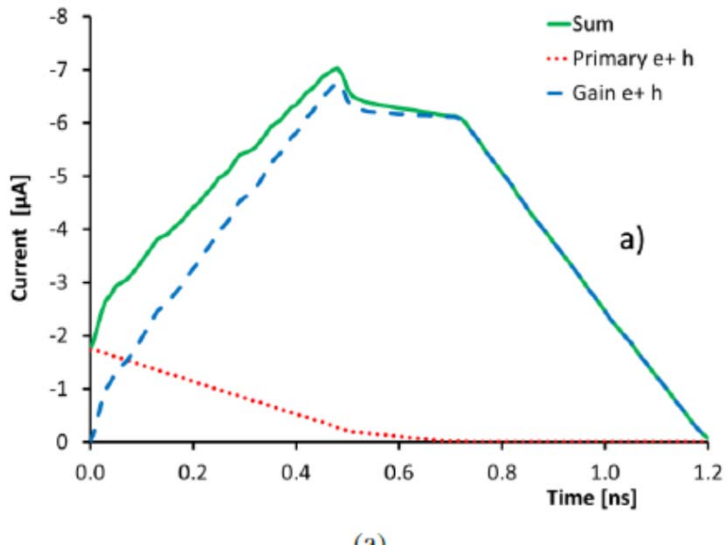
Optimise the number of hits per track

Sensors R&D activity

with strong interaction with RD50 and some CMS colleagues

LGAD first principles





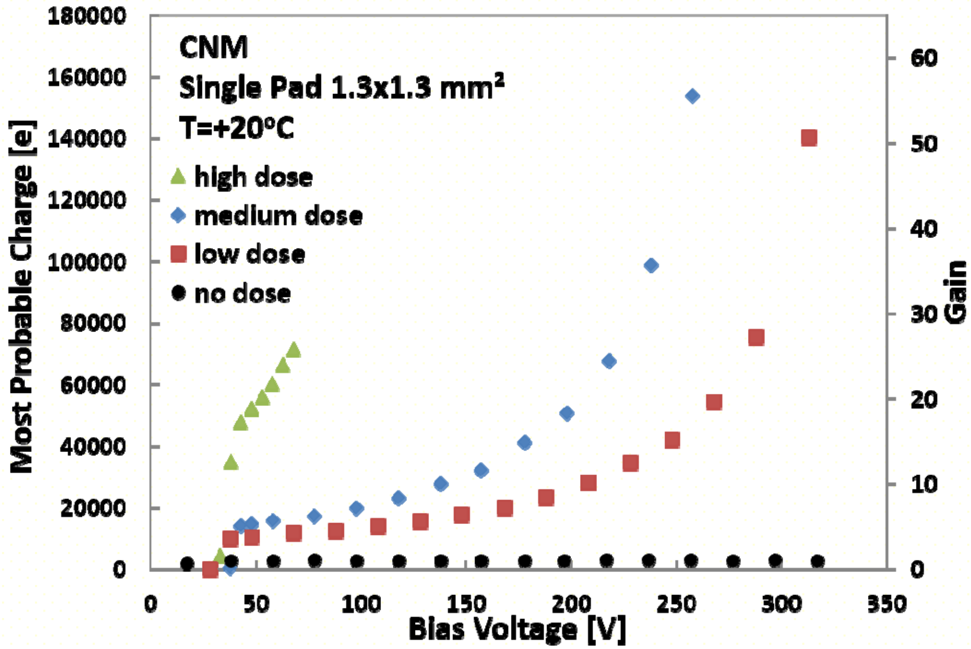
Low Gain Avalanche Diode pioneered by CNM.
Now produced by HPK and FBK with similar performance (except breakdown values)
BNL and Micro in near future
A lot of work also done within RD50

Gain (charge ratio of LGAD/diode) : (→ S/N)
- moderate gain (10-50) provided by thin highly doped avalanche region (a few μm with high electrical field, ~a few 100 kV/cm)
- depend on doping density
- independent of sensor thickness

Signal speed : (→ t_{rise})
- Not very fast, rise time around 0.5-0.6 ns
- Rise time and duration depends on sensor thickness

Gain versus bias voltage

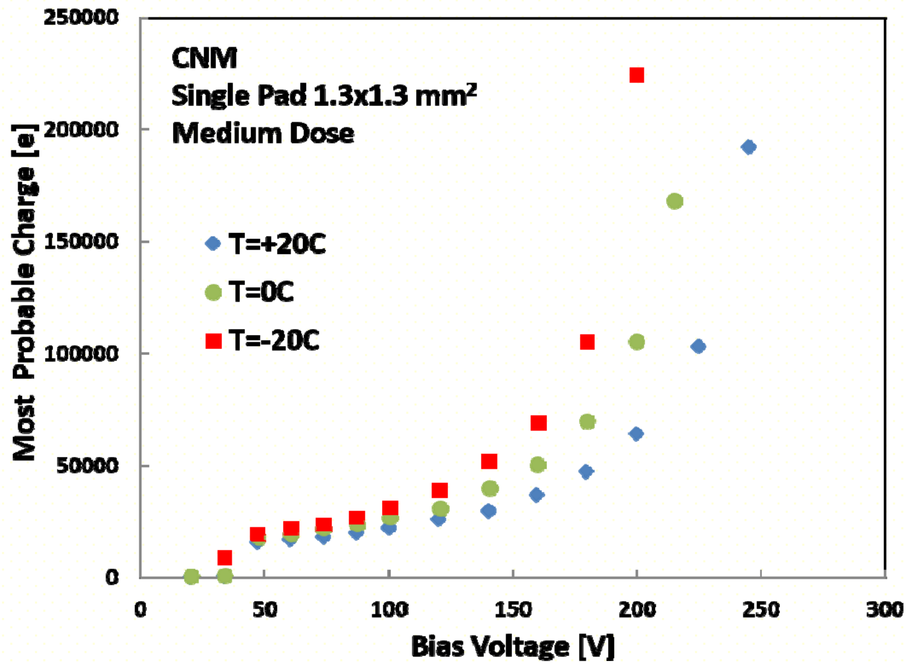
varying doping



Breakdown voltage before irradiation quite sensitive to doping level (2.0, 1.9, 1.8 10^{13} cm^{-2})

→ gain of 20 reached easily

varying temperature



Operate at low temperature (target in ATLAS near –30 °c)

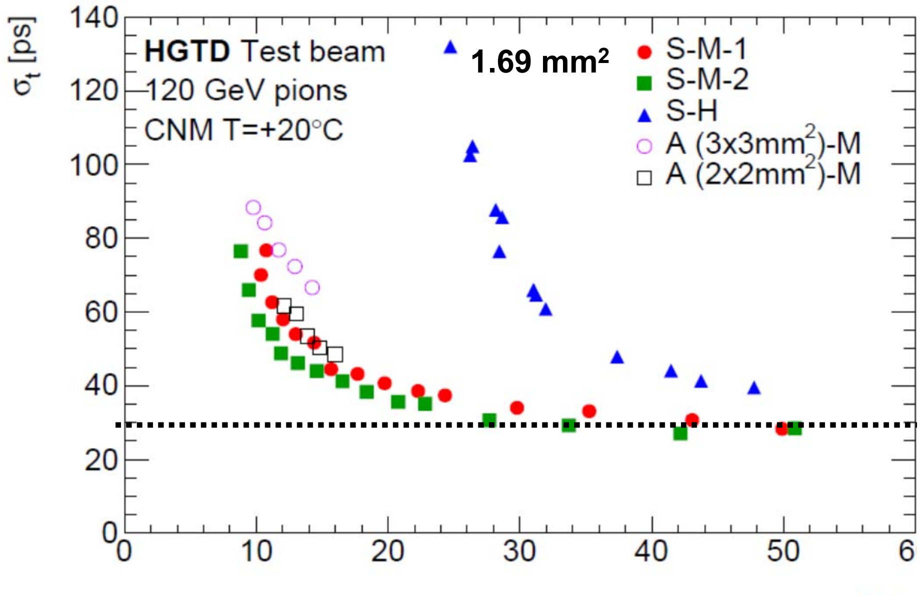
→ Gain x 2-3

→ Reduce operation voltage

→ Reduce current leakage after irradiation

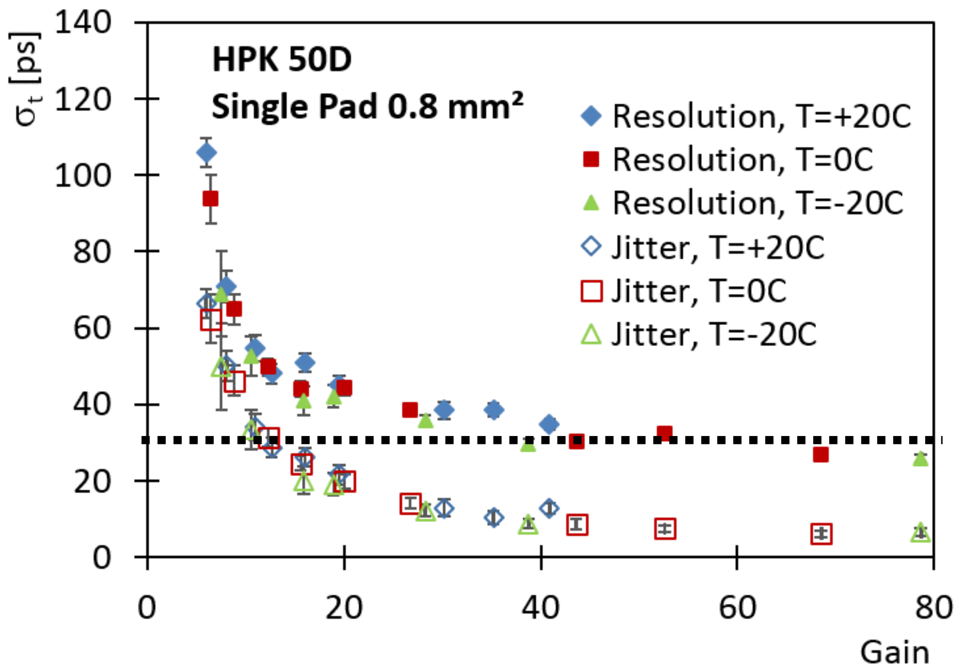
Time resolution versus gain

CNM Sensor at room temperature



https://arxiv.org/abs/1804.00622

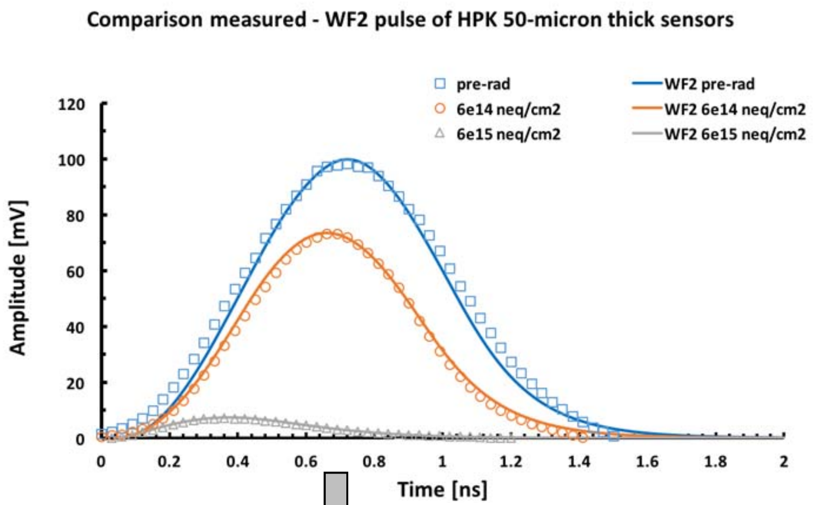
HPK Sensor from +20 to –20 °c

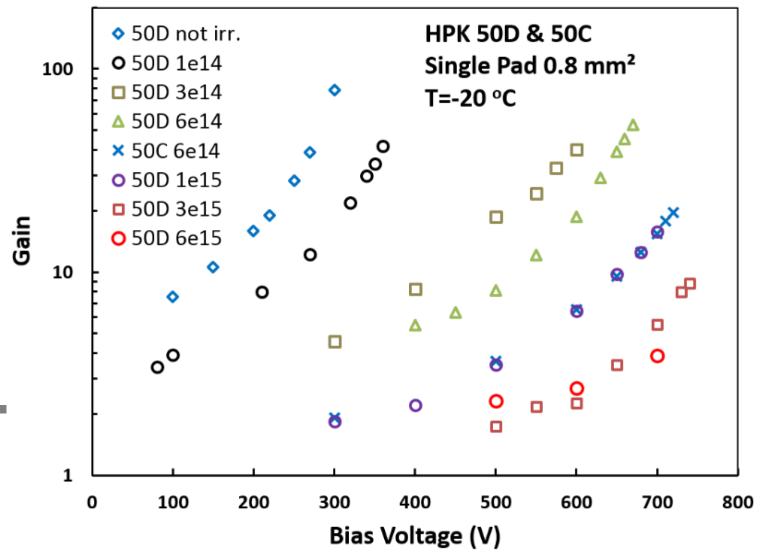


Similar time resolution for CNM/HPK with ultimate time resolution of 30 ps for 50 μm thickness, limited by "Landau" term

(measurements done with discrete, quite power dissipative, electronics sampling the signal (no TDC))

Sensors gain with irradiation



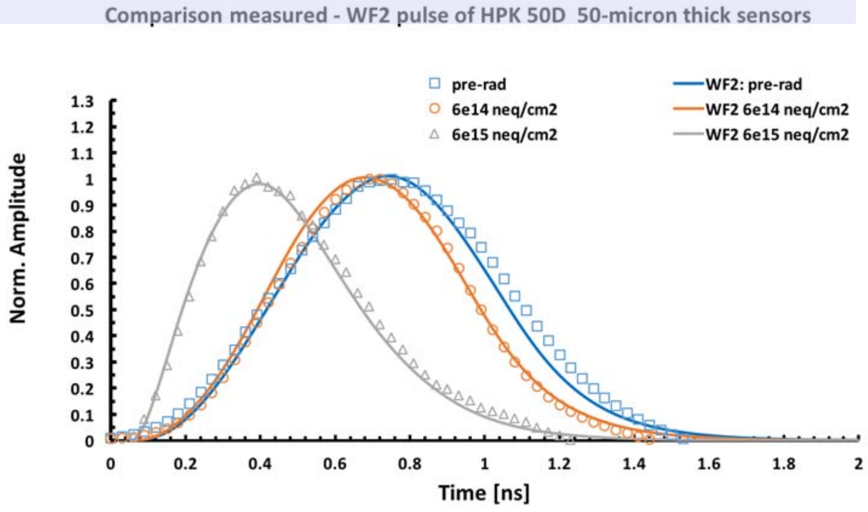


With irradiation up to 1.10^{15} neq/cm^2
- Degradation of gain due to loss of effective doping in avalanche region, slightly faster signals

→ partially mitigating by increasing bias voltage

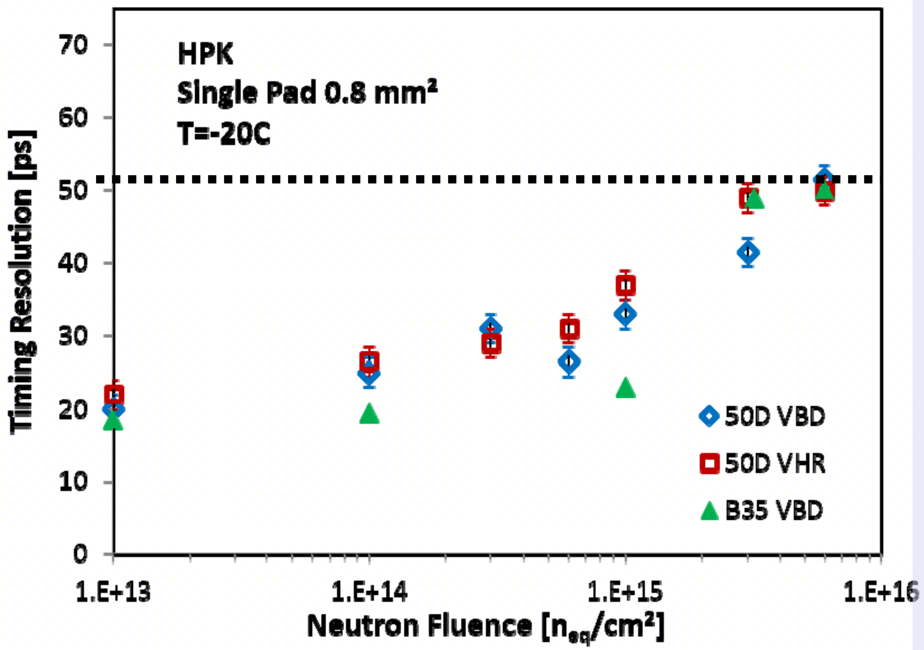
For fluence > 1.10^{15} neq/cm^2 still some gain from the bulk region, and faster signal

With proton irradiation, slightly smaller effect



Z. Galloway et al, arXiv:1707.04961

Sensors time resolution with irradiation

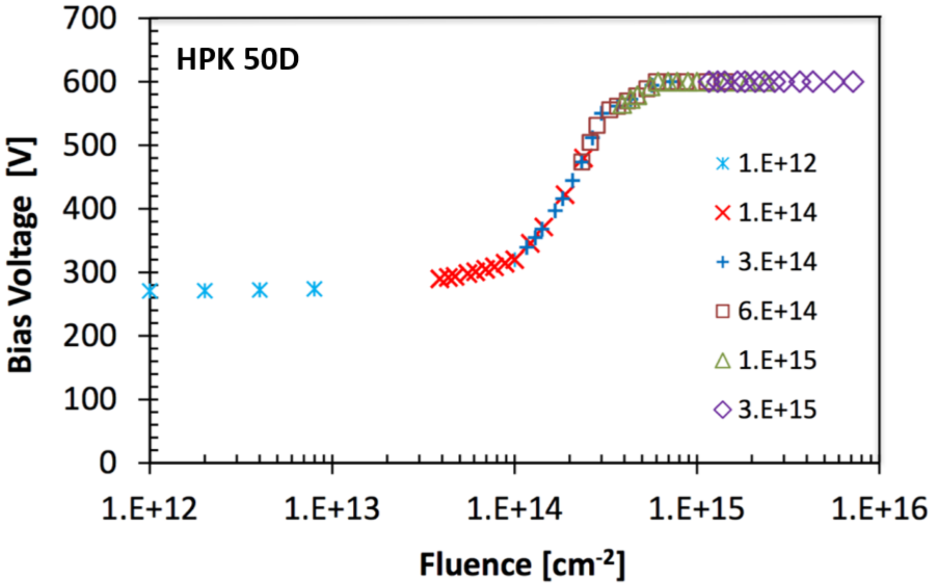


Time resolution smaller than 50 ps up to ~5. 10^{15} neq/cm^2 with bias voltage (VHR) 10 % below breakdown voltage (VBD)

35 µm thickness :

- a bit better than 50 µm below 1 10^{15} neq/cm^2, but similar at high fluence
- Smaller operating voltage
- But larger capacitance will make hard to achieve this performance with ASIC

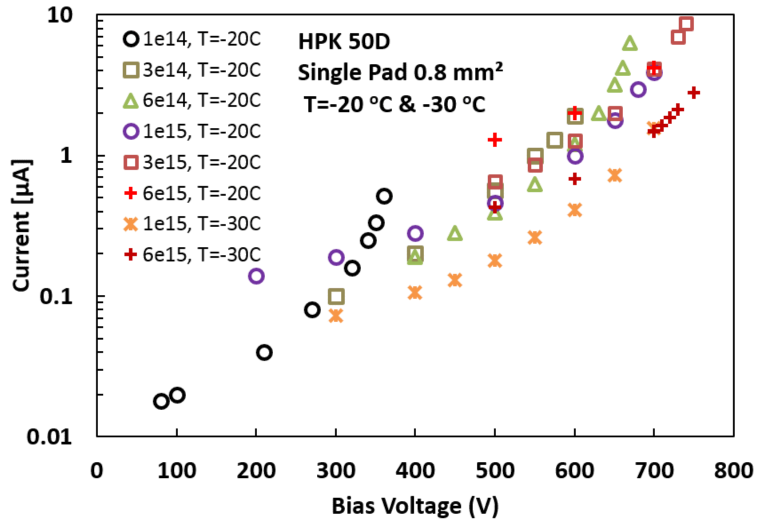
Bias voltage operation

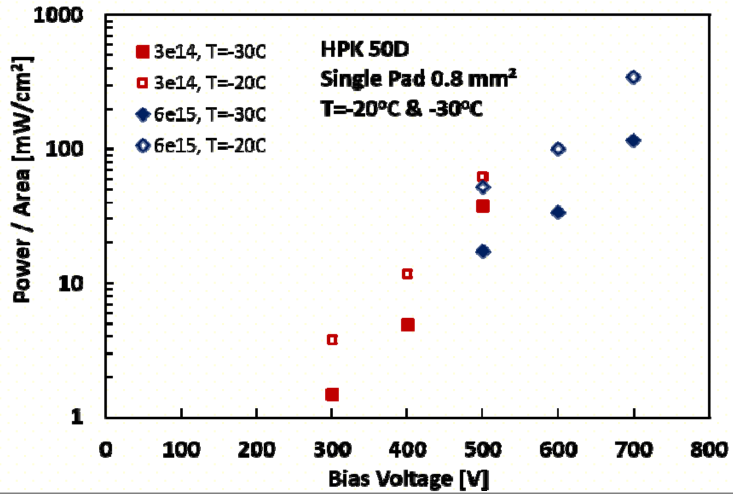


Bias voltage to be adjusted as function of time (fluence) monitored by TOT and leakage current measurement

In current design, individual bias voltage per sensor (2 cm along X or Y direction)

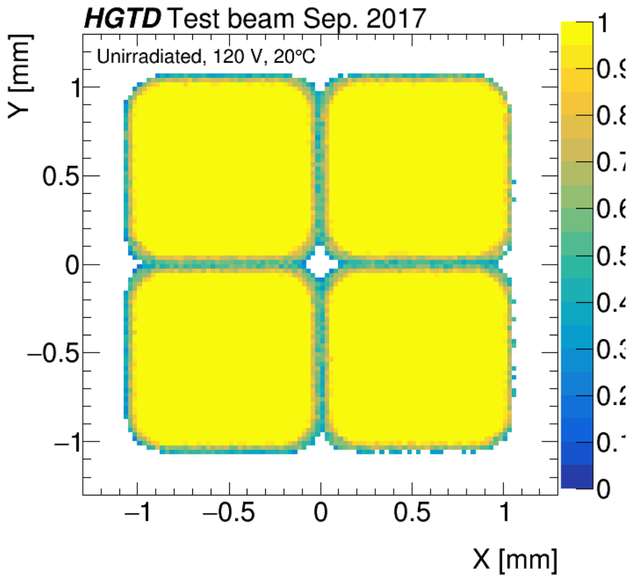
Leakage current

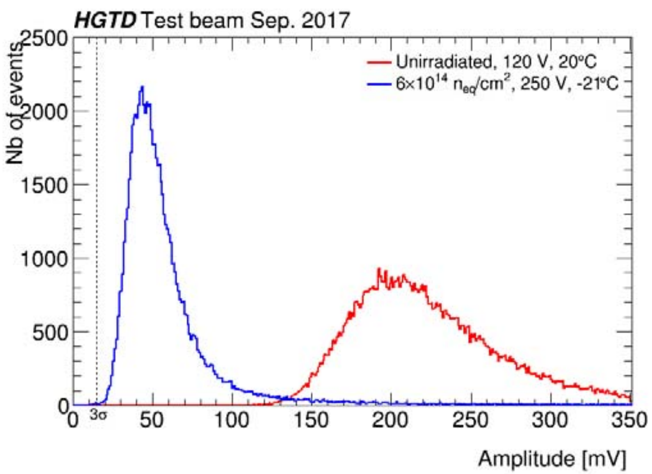


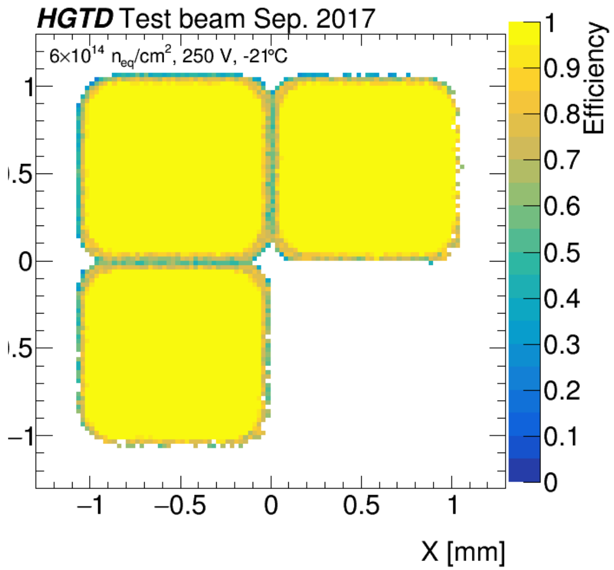


Power dissipation dominated by ASIC

Preliminary pad array measurements



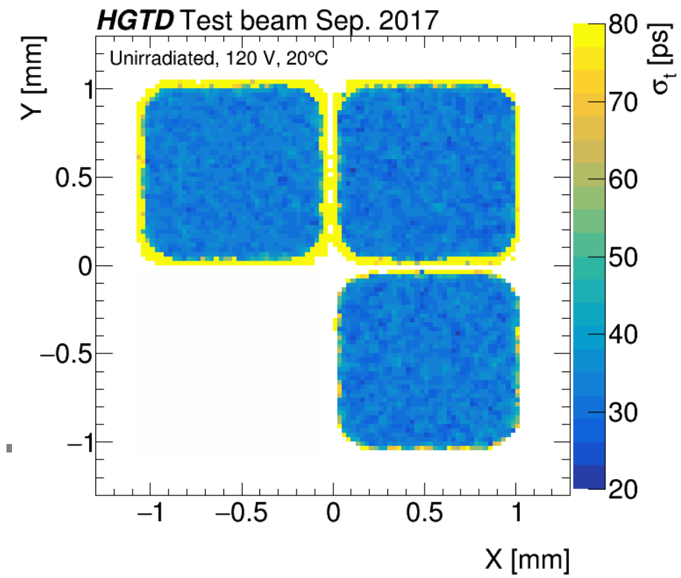


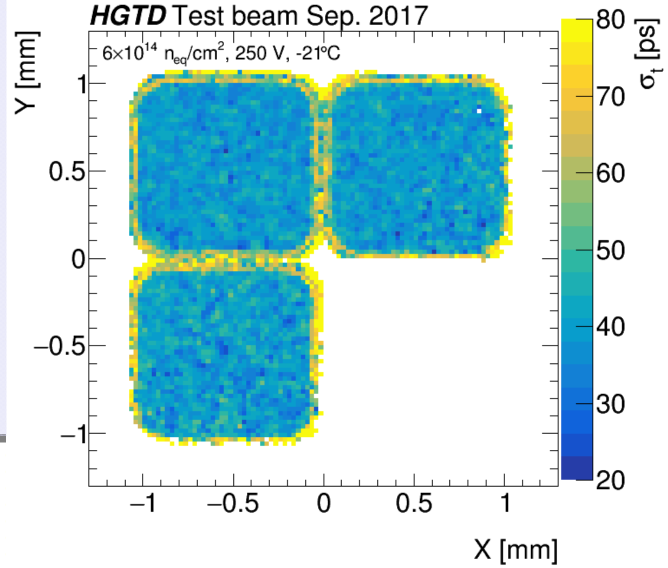


Up to 1. 10^{15} neq/cm^2 , can achieve
S/N > 10
Efficiency > 98-99%

Beyond on going study

Time resolution uniform within pads





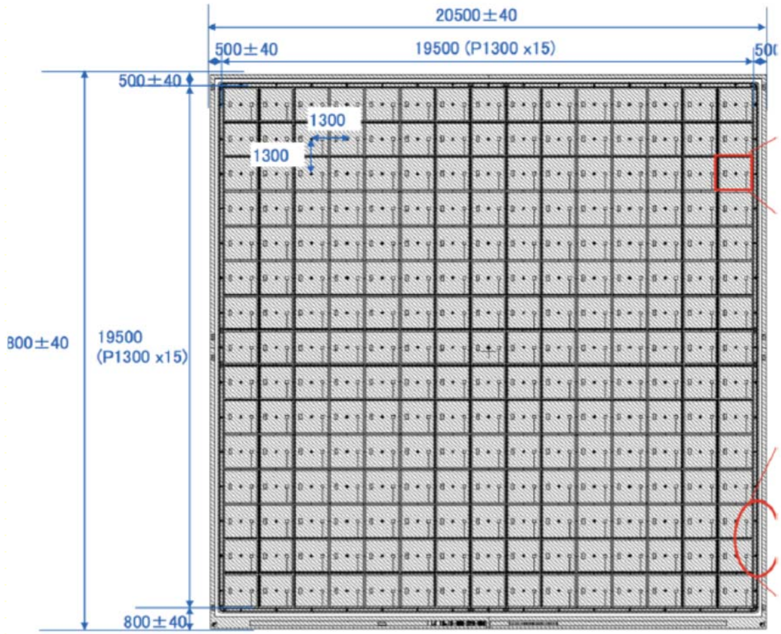
Main sensors R&D in 2018/2019

Test of sensors with Carbon spray in the bulk

Production of similar sensors structure and arrays (up to 2x2 cm^2) by CNM and HPK

Optimisation of fill factor (inter pad distance from 50 → 100 μm)

Integrated sensor + ASIC measurements



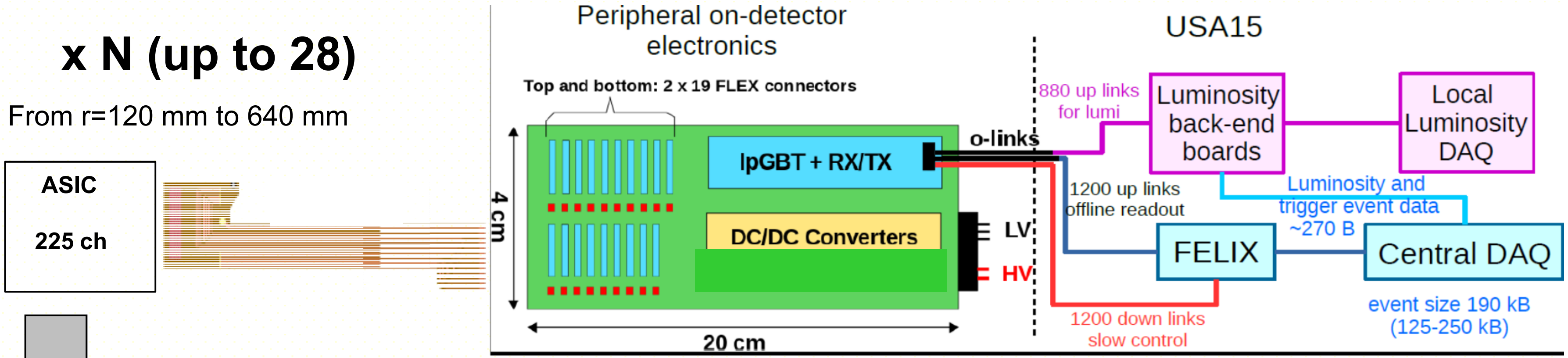
Electronics R&D activity

Electronics read- out overview

From r= 740 mm to ~940 mm

x N (up to 28)

From r=120 mm to 640 mm



Electrical transmission over up to 75 cm at 320 Mb/s to 1.28 Gb/s

Quite similar problematic than other ATLAS/CMS detectors

ASIC ALTIROC specific to HGTD

ASIC requirements

Pad size	1.3×1.3 mm^2
Detector capacitance	3.4 pF
TID and neutron fluence	Inner region: 4.1 MGy3.7×10^{15} n_{eq}/cm^2 Outer region: 1.6 MGy, 3.0×10^{15} n_{eq}/cm^2
Number of channels/ASIC	225
Collected charge (1 MIP) at gain=20	9.2 fC
Dynamic range	1-20 MIPs
(preamplifier+discr.) jitter at gain = 20	$<$ 20 ps
Time walk contribution	$<$ 10 ps
TDC binning	20 ps (TOA, TZ TOT), 40 ps (VA TOT)
TDC range	2.5 ns (TOA), 5 ns (TZ TOT), 10 ns (VA TOT)
Number of bits / hit	7 for TOA and 9 for TOT
Luminosity counters per ASIC	7 bits (sum) + 5 bits (outside window)
Total power per area (ASIC)	$<$300 mW/cm^2 ($<$1.2 W)
e-link driver bandwidth	320 Mb/s, 640 Mb/s or 1.28 Gb/s
Latency for L0/L1 triggering	10/35 μs

Challenging radiation level, choose TSMC 130 nm CMOS

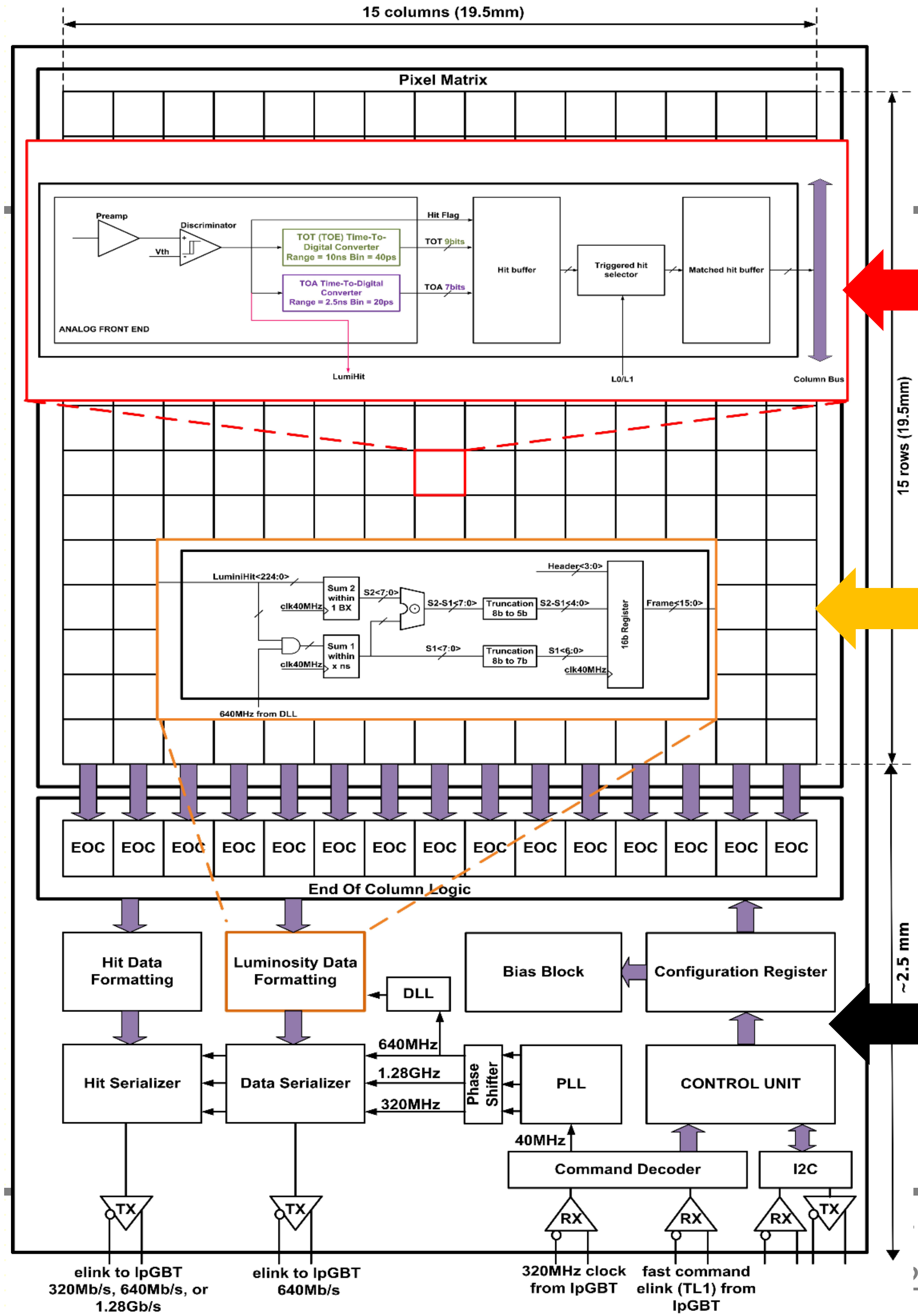
Challenging timing resolution for small charge

Keep acceptable power dissipation for CO2 cooling

Cope with both ATLAS trigger scheme

And quite reduced time for ASIC R&D…

ASIC architecture



225 pixel read-out channels (at prototype level)

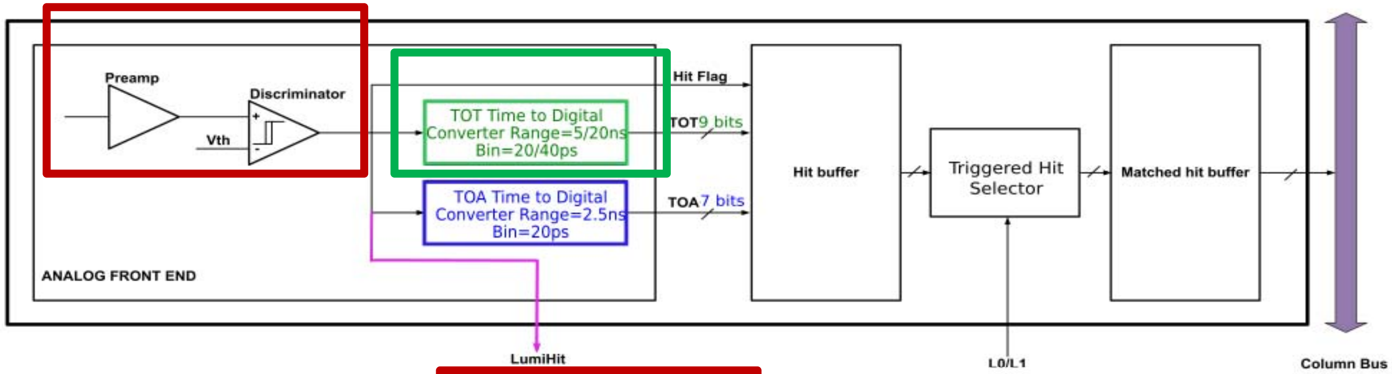
A luminosity data formatting block

Quite standard off-pixel detector matrix read-out (still at design phase)

Tuneable speed serializers

Phase shifter for the clock with ~100 ps accuracy

Pixel architecture



$$\sigma^2_{\mathrm{elec}} = \sigma^2_{\mathrm{jitter}} + \sigma^2_{\mathrm{TW}} + \sigma^2_{\mathrm{TDC}}$$

Given by preamplifier and discriminator performance + TOT correction

Given by TOA TDC lsb = 20 ps so expect contribution < 6 ps

Preamplifier design

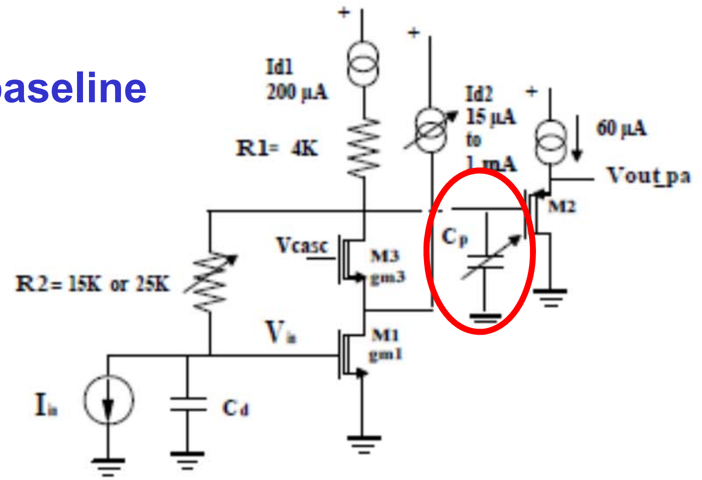
$$\sigma_{jitter} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}}\sqrt{\frac{tr_a^2 + t_d^2}{2tr_a}} = \frac{C_T}{Q_{in}}\sqrt{\frac{2kTt_s}{g_m}},$$

→ No need of infinitely fast preamplifier. Preamplifier rise-time (tr_a) matched to LGAD rise-time t_d : $tr_a = t_d = t_s$ in the range 0.5-1 ns

→ Optimise t_s and g_m (using relatively large transistors and currents)

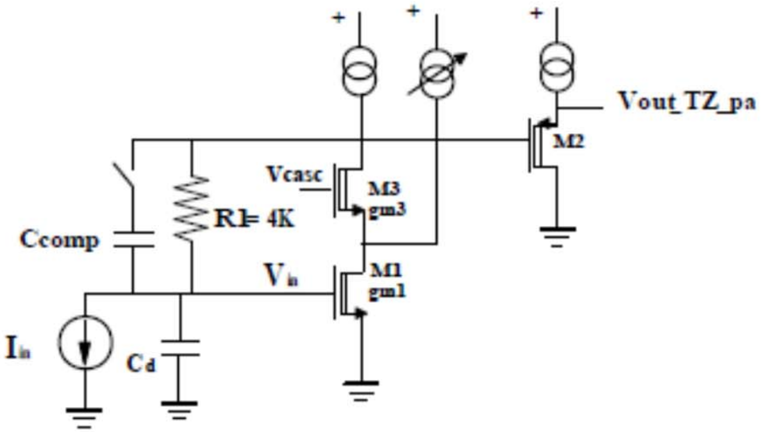
Broadband preamplifier with common source (VA)

baseline



(a)

Pseudo-Trans-impedance amplifier (TZ) similar as Test Beam design wtih discrete components and larger current



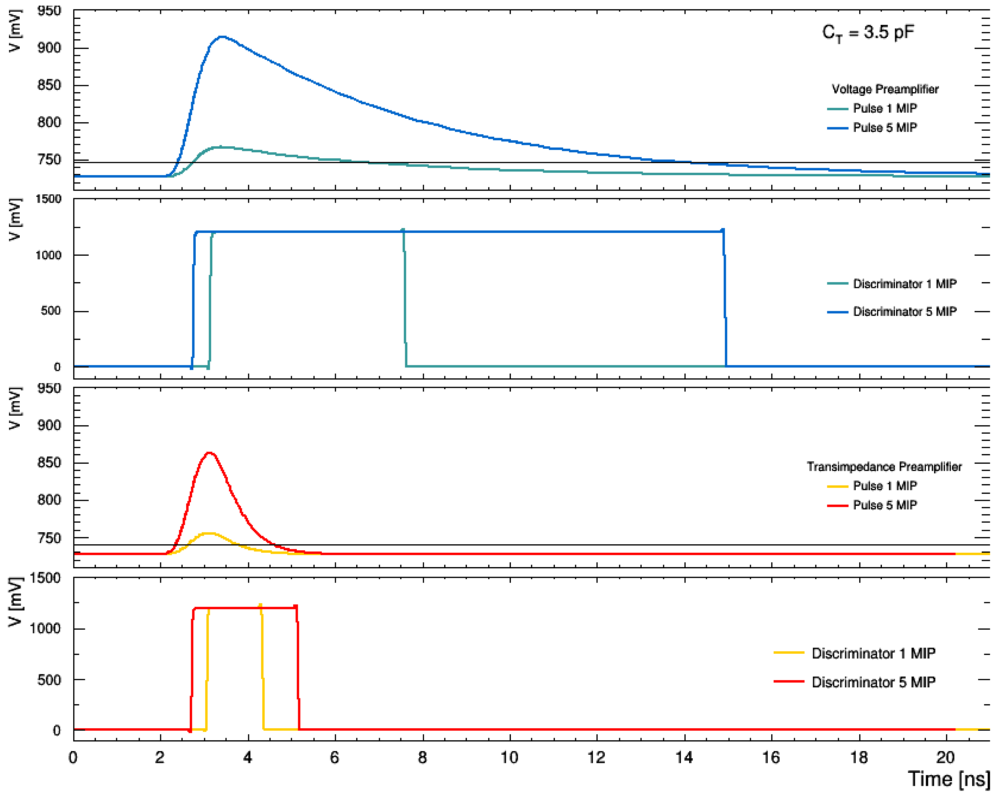
(b)

Proto ALTIROC0-V1 (2017) and V2 (2018)

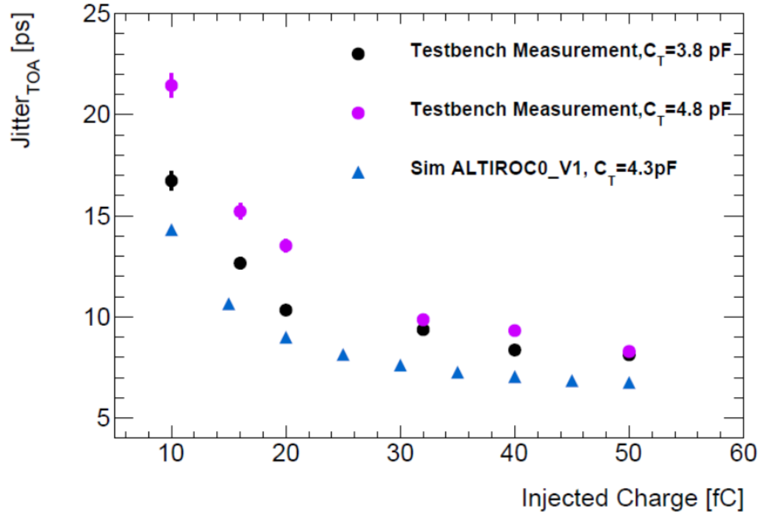
Only in V2 (2018)

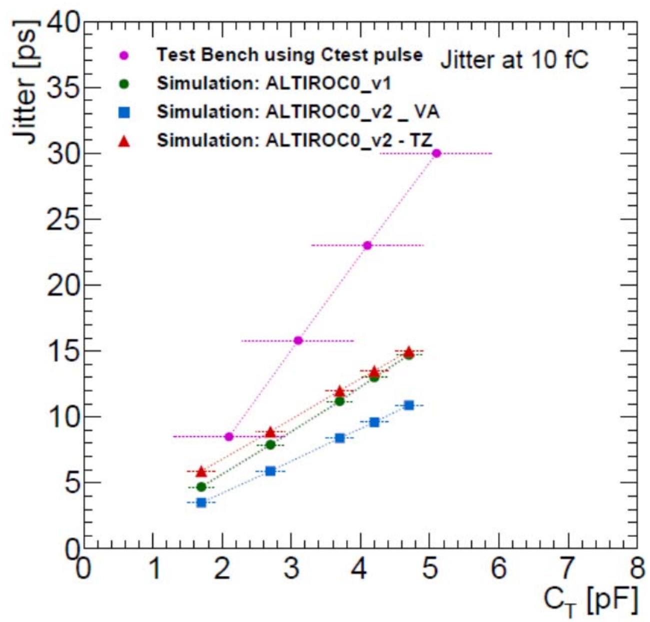
Preamplifier performance

Waveform output

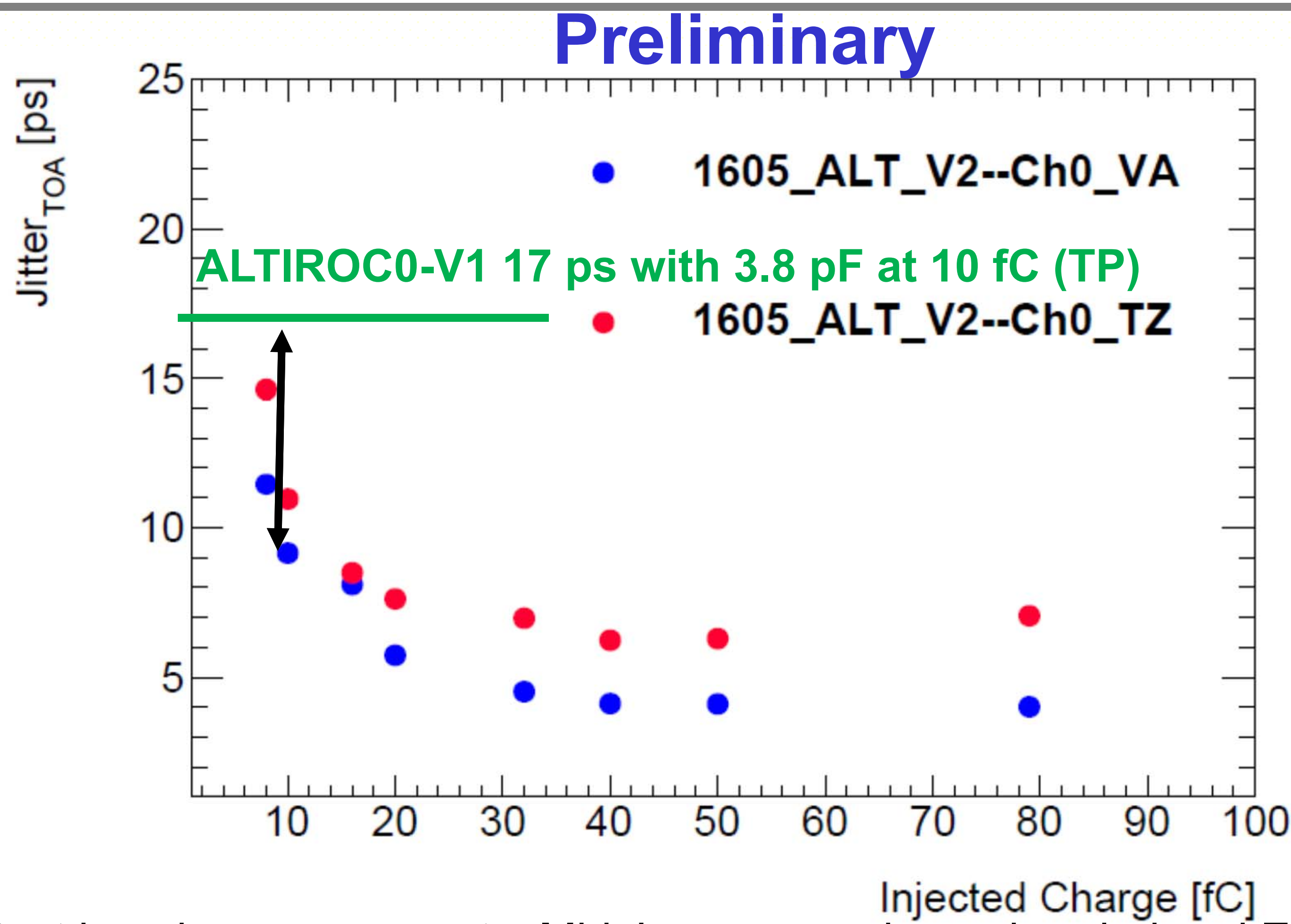


TZ width / TOT shorter





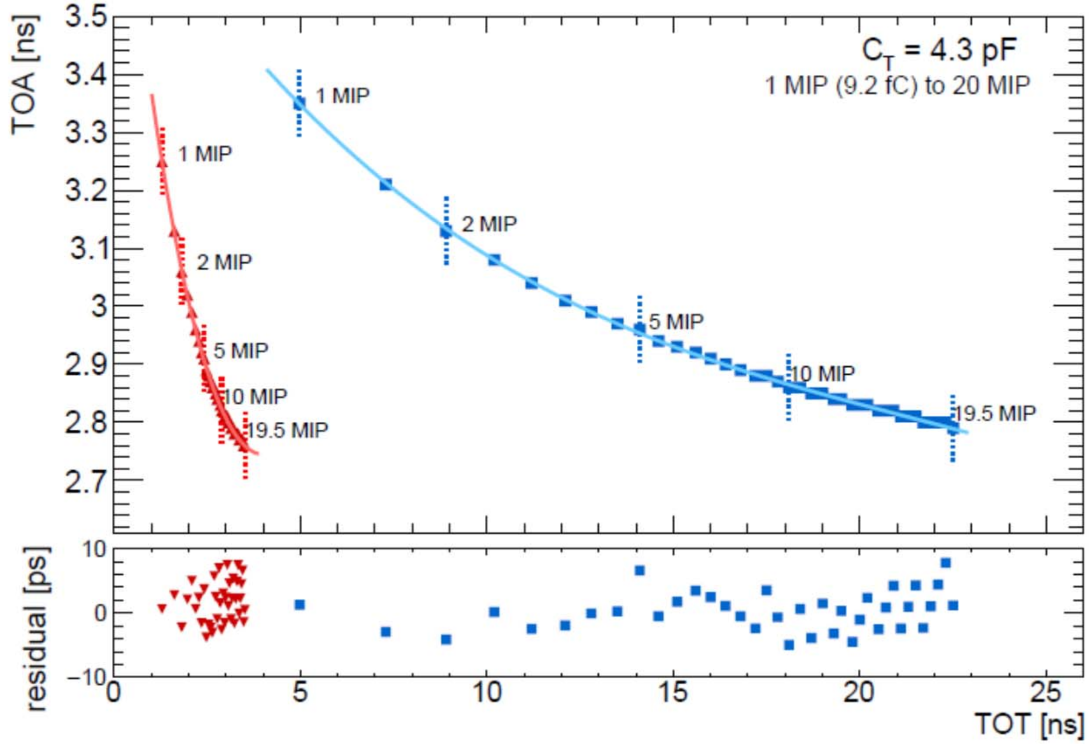
ALTIROC0-V2 : VERY preliminary measurements



On going test bench measurements. Mid June sensor bump bonded and End June beam test at CERN

Time Walk correction

Use TOT as estimator of amplitude to correct for time walk effect



$$\sigma_{\mathrm{TimeWalk}} = \left[\frac{V_{\mathrm{th}}}{\frac{S}{t_{\mathrm{rise}}}}\right]_{\mathrm{RMS}} \propto \left[\frac{N}{\frac{dV}{dt}}\right]_{\mathrm{RMS}}$$

After correction, peak to peak variation < 20 ps so contribution to < 10 ps to resolution
TZ fast dependence implies a 20 ps lsb for the TOT measurements, while VA can be 40 (80) ps

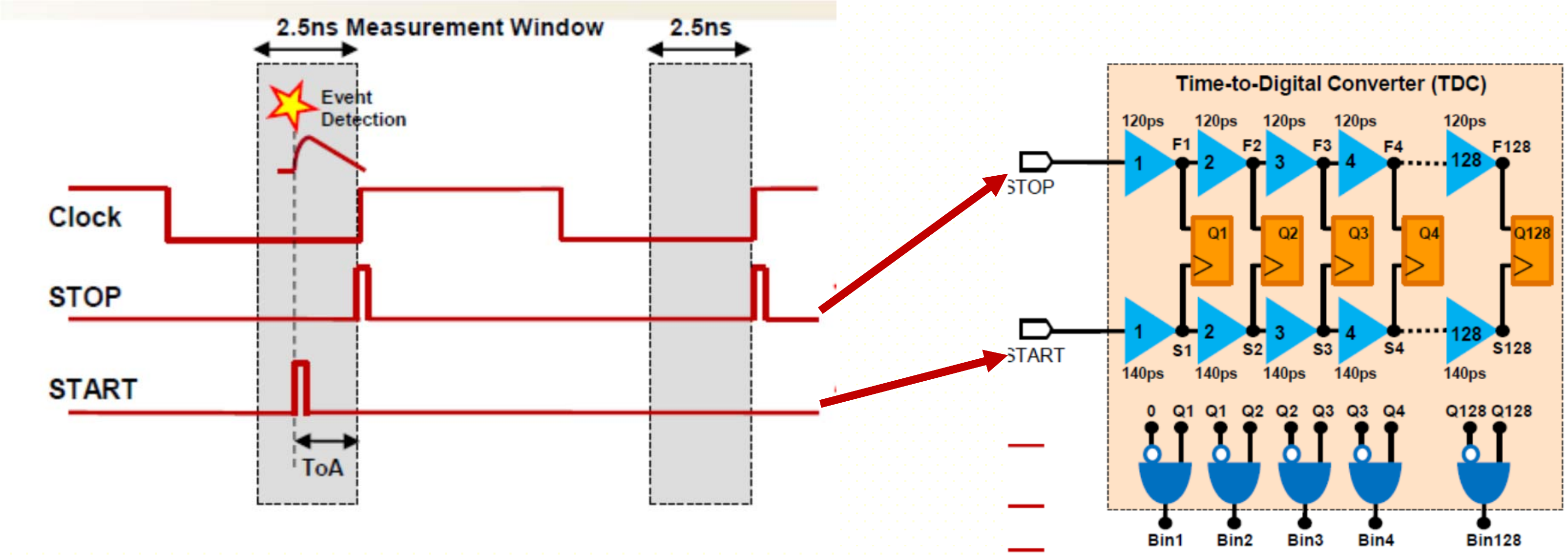
Time to Digital Converter (TDC) for TOA

Vernier delay configuration with two delay lines :

- Time resolution (20 ps) = difference in the delay of the cells in each line **slow** (140 ps) and **fast** (120 ps) lines
- Time measurement (TOA) only over 2.5 ns window centered on bunch crossing

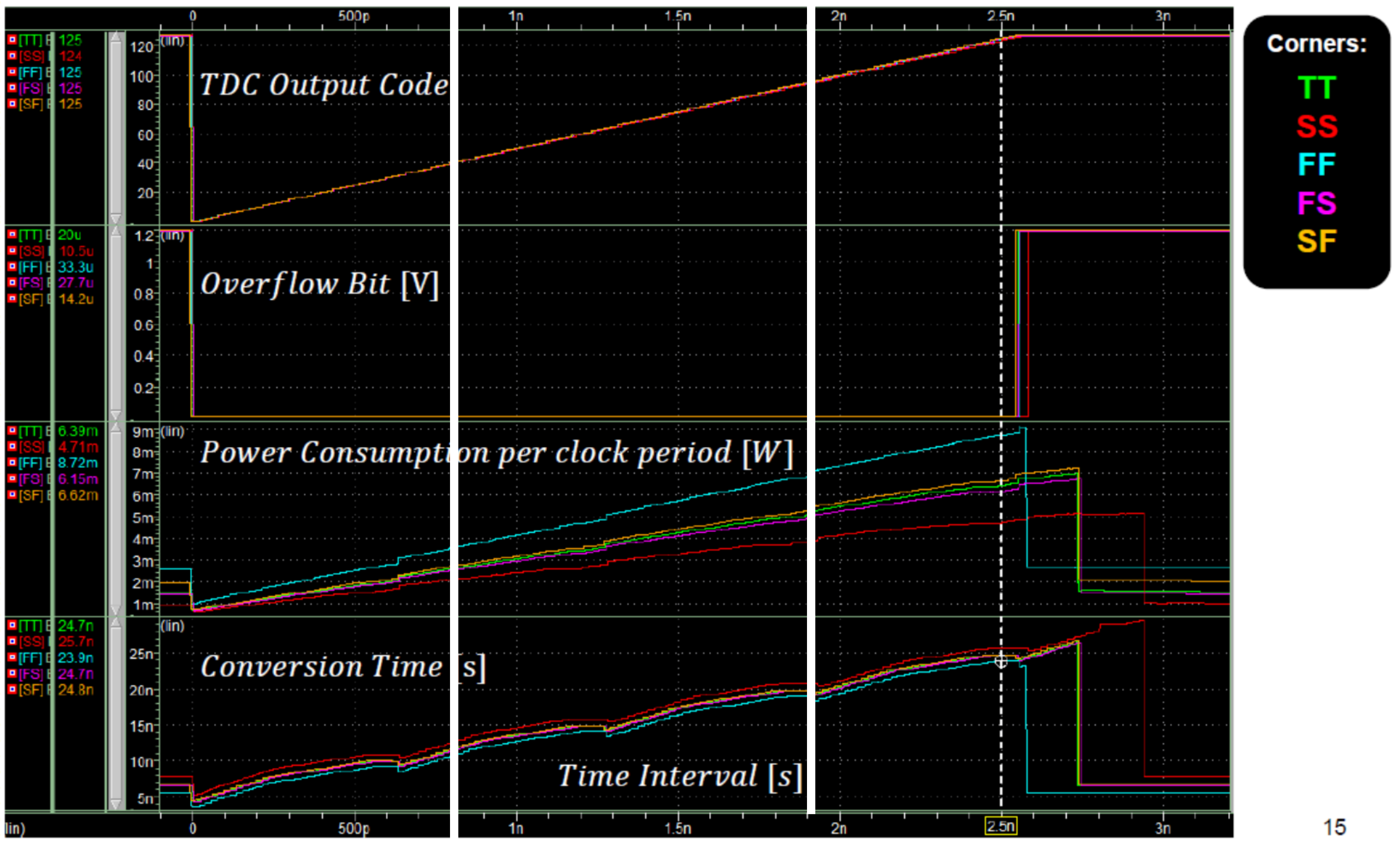
TOA given by the number of stage needed to have the STOP to surpass the START

- No power consumption if not hit.



TOT TDC made of a Coarse delay line + TOA TDC

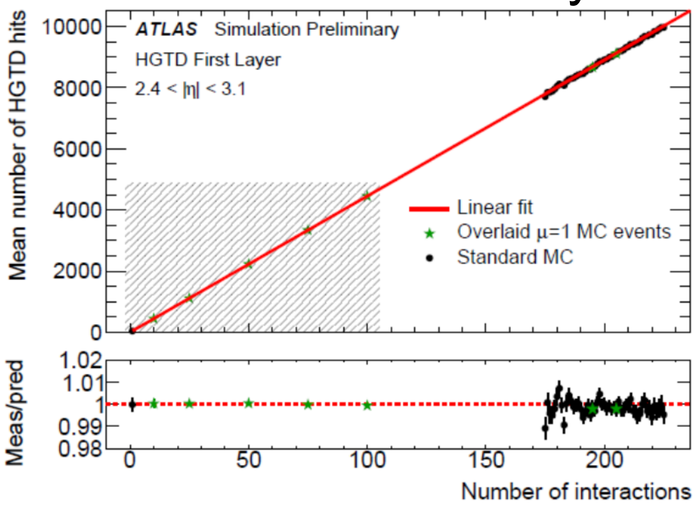
Time to Digital Converter (TDC)

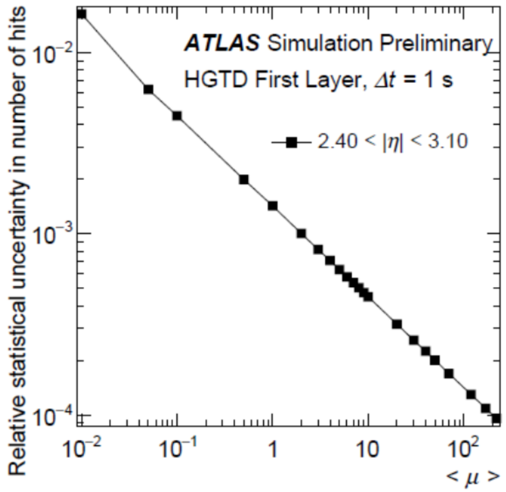


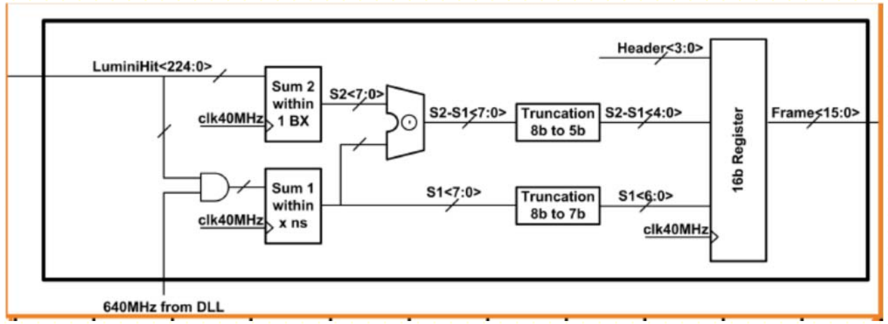
Most of the hit in time within central window → power consumption 5 mW x occupancy
Conversion still to be optimized to stay within 25 ns

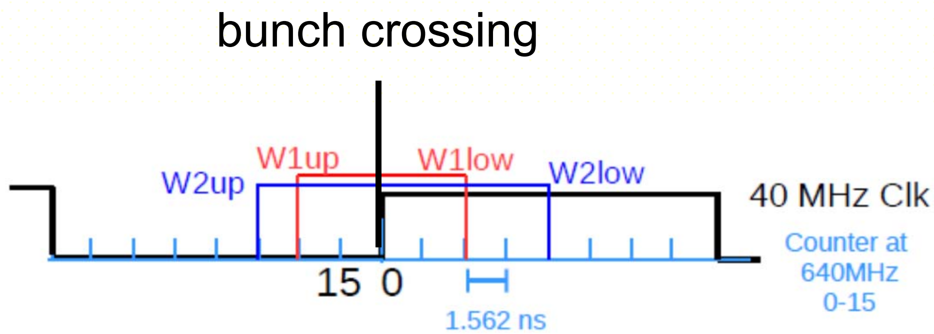
Luminosity counters

HGTD can easily provide an instantaneous luminosity



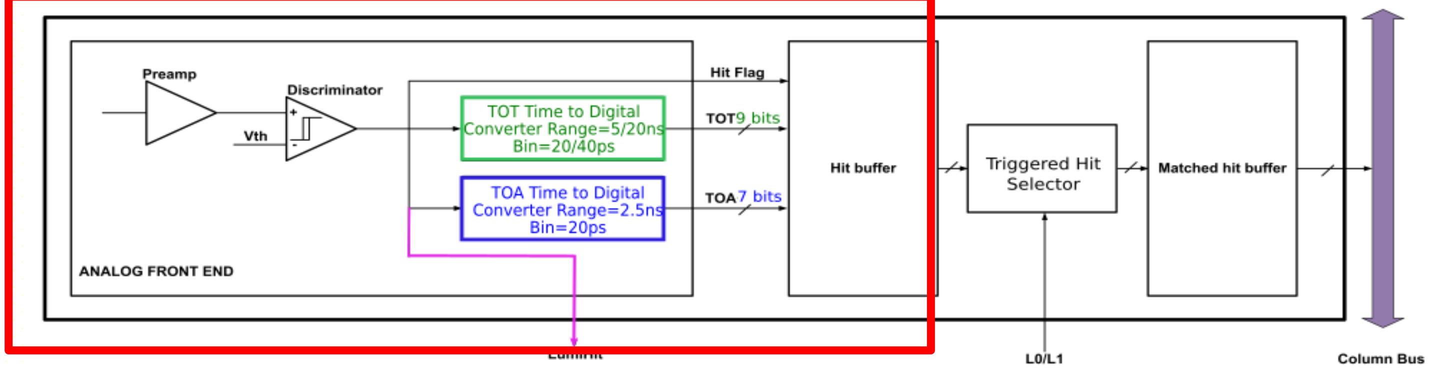




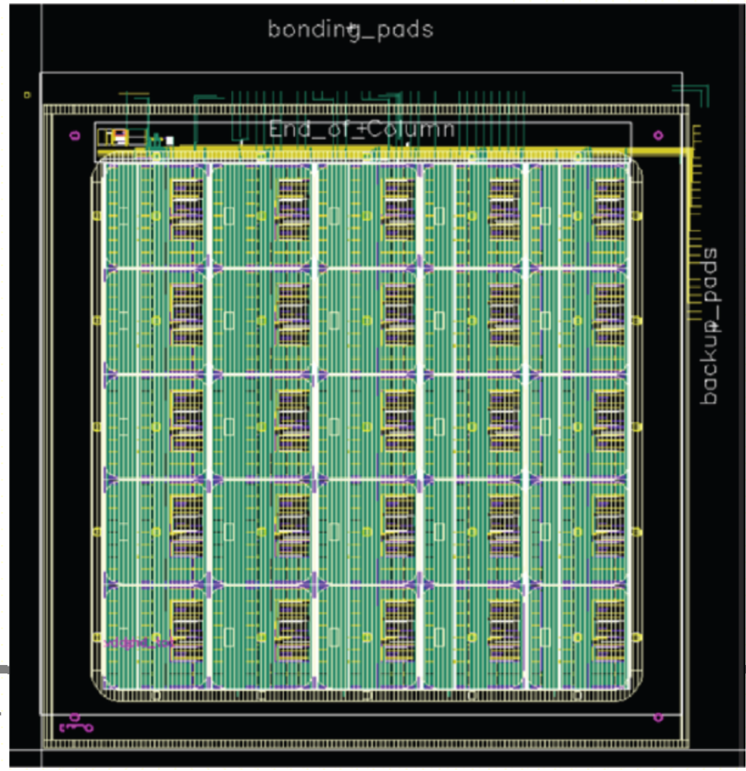


For each ASIC,
- compute number of hits in two windows centered on bunch crossing
- transmit in time and out-time numbers of hits at each bunch crossing

ALTIROC1

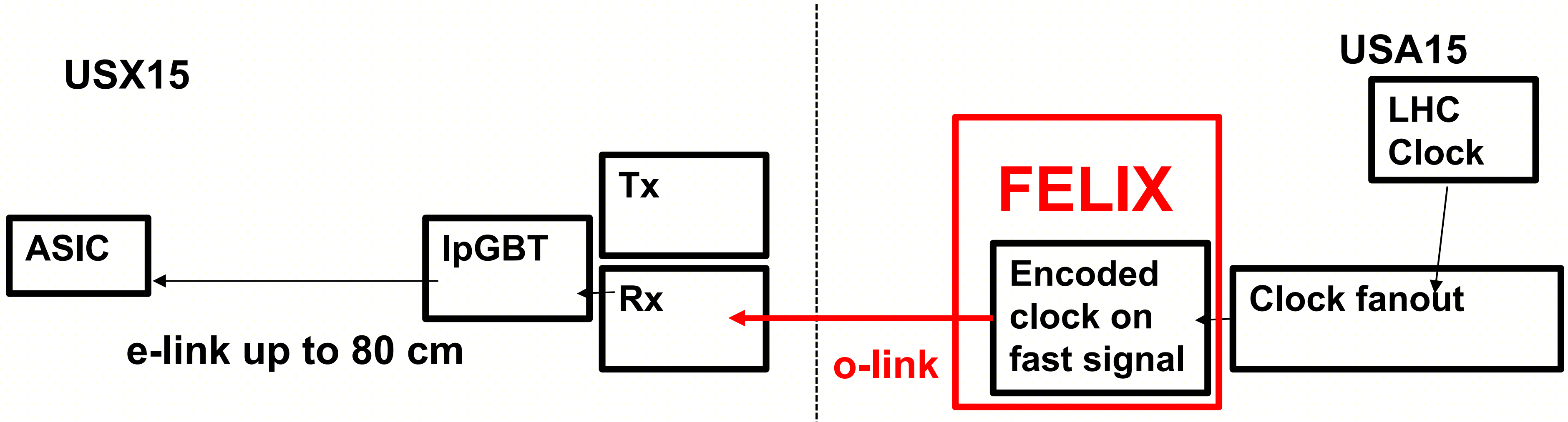


25 channels chip with preamplifier (VA or TZ) + discriminator + TOA and TOT (TDC) and local memory
Include prototype of final clock distribution in ASIC for 16 channels
Layout finished, post simulation ongoing
Submission on June 13 th
Might include an independent block with phase shifter if ready



Clock distribution and t_0 calibration

Clock distribution to ASIC : jitter



Baseline design is to transmit the clock encoded through the lpGBT

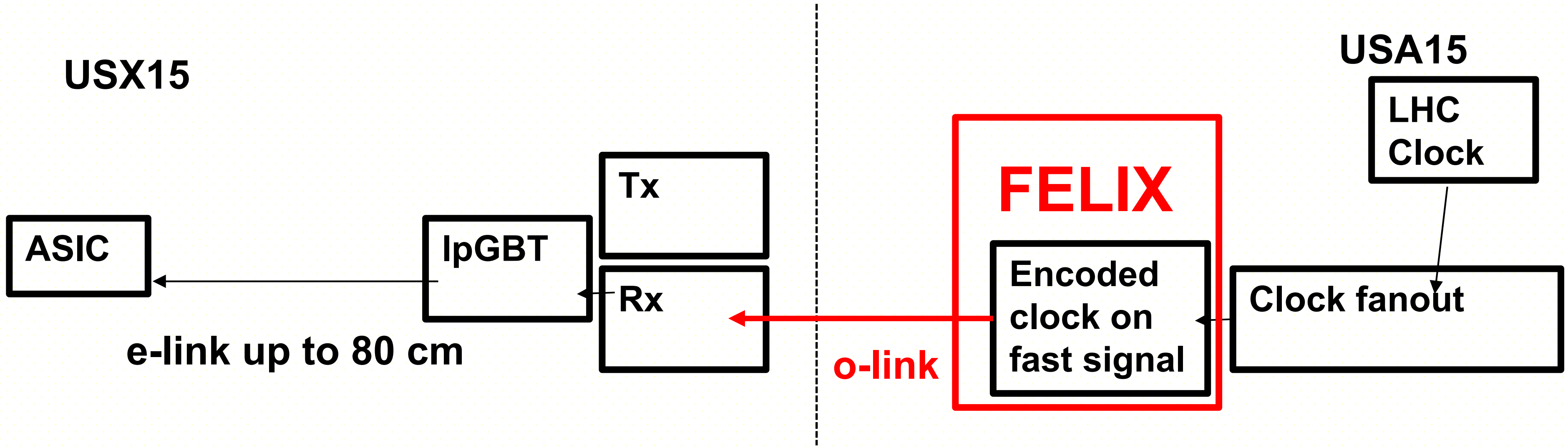
→ Clock contribution to time resolution relies on expected lpGBT jitter < 5 ps and FELIX contribution : total < 10 ps ?

→ Might clean it in ASIC (PLL)

→ Providing a clock directly through dedicated links quite difficult for services

Work started within the ATLAS/CMS common working group set-up by CERN-EP-ESE-BE (S. Baron)

Clock distribution to ASIC : wander



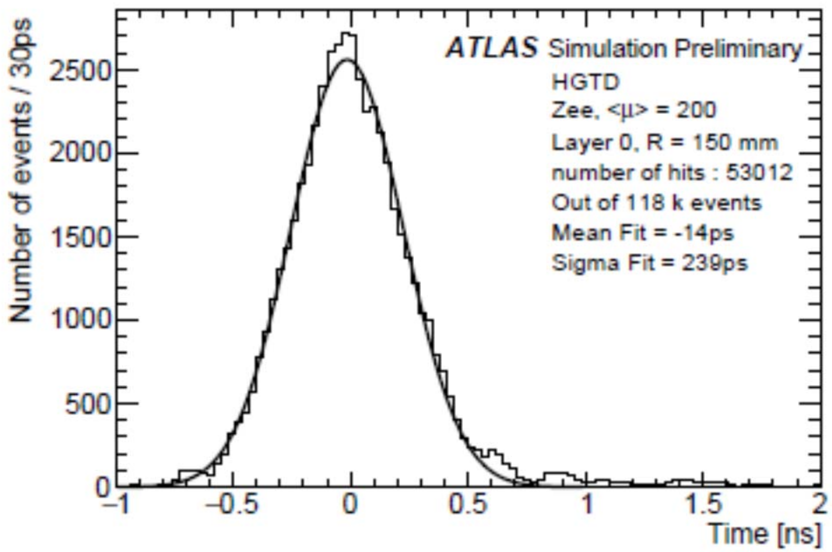
Phase shifter in ASIC only used to align coarsely the measurement window (~100 ps accuracy)

t_0 of each channel needs to be calibrated to a few ps :

- different path length for signal, time of flight → calibration signals
- "Low frequency" clock phase variation with time/temperature → wander

→ use data to compute/correct online/offline the possible t_0 variations

T0 calibration with data



Inclusive hit time distribution in a pixel : rms 240 ps

→ Can measured t_0 of pixel to better than 5 ps with 10000 hits

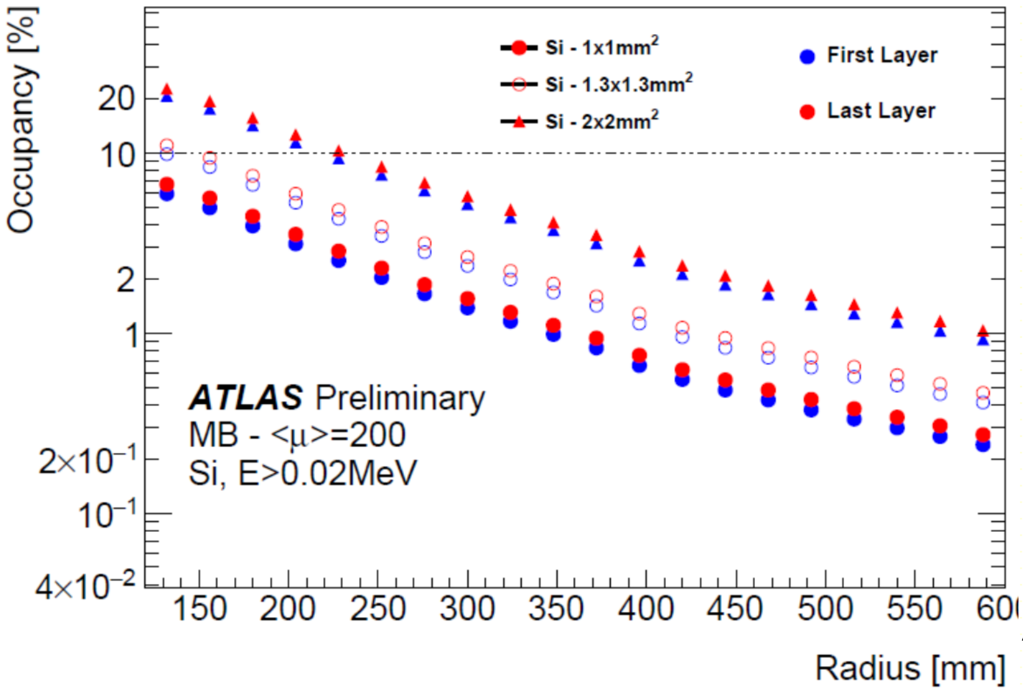
Taken into account occupancy, it corresponds to 10^5 events at inner radius and 10^6 events at higher radius

		In Felix board data at 1 MHz,	offline data at 10 kHz
Inner radius	per channel	0.1 s	10 s
Outer radius	per channel	1s	100 ps
Per ASIC	(inner/outer)	0.4/4 ms	

→ Could correct low frequency variation up few kHz frequency

Layout optimisation and design

Sensor pad size



Pad size is a trade-off between

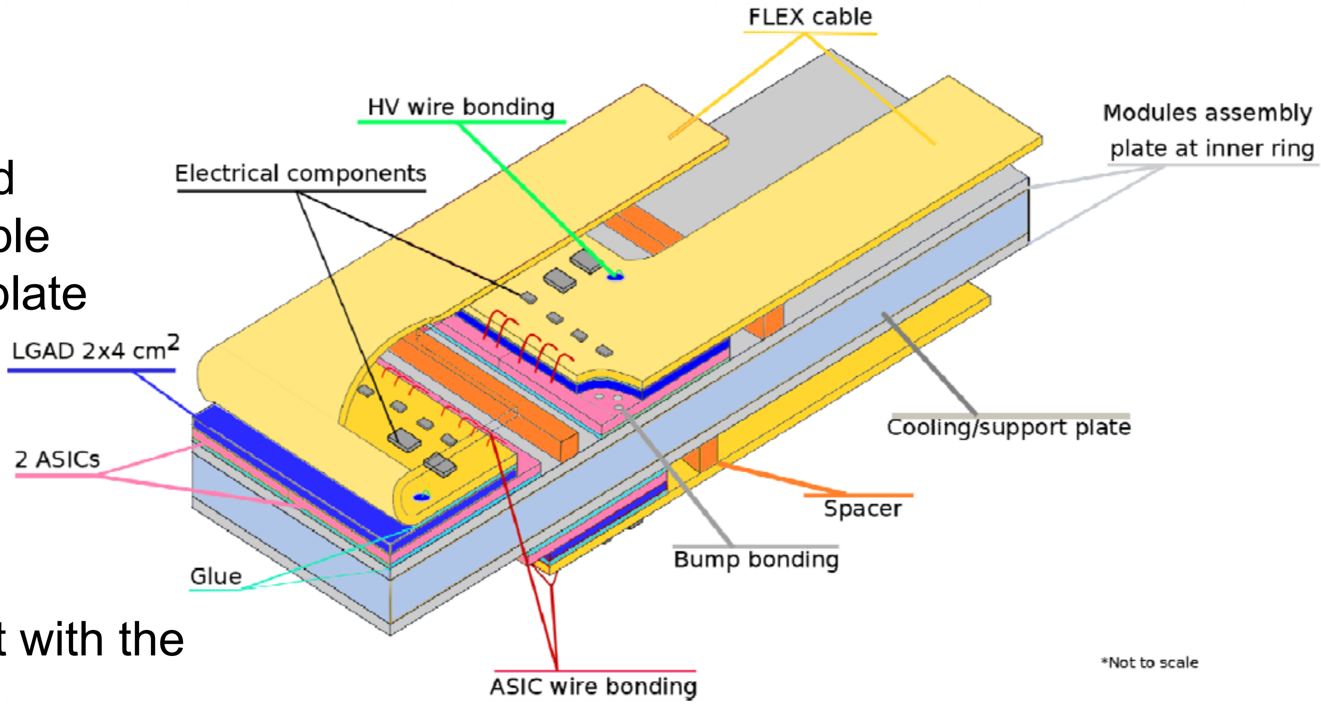
- Occupancy and time resolution (capacitance) → small pads
- Efficiency (fill factor) and channel density (power consumption) → large pads

Baseline is a unique sensor pad size of 1.3 x 1.3 mm^2

All sensors identical (4x2 or 4x4 cm^2)

HGTD Module and stave

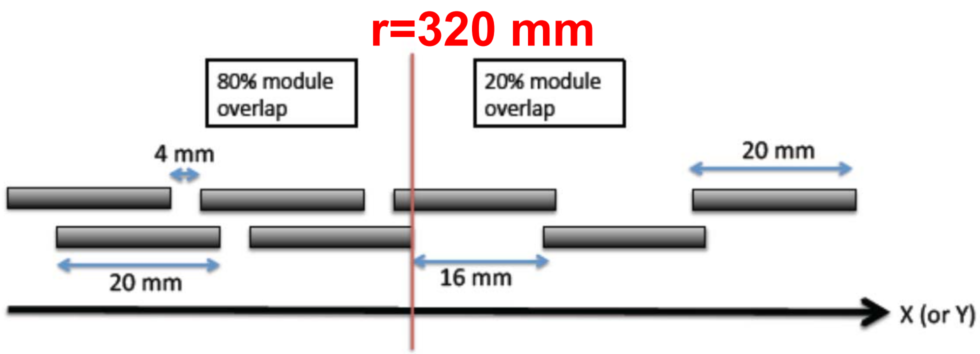
7888 modules :
- 4x2 cm^2 sensor
- Two ASIC bump bonded
- Wire bonding to flex cable
- Glued on intermediate plate along X or Y direction



Double sided sensor layert with the cooling plate between

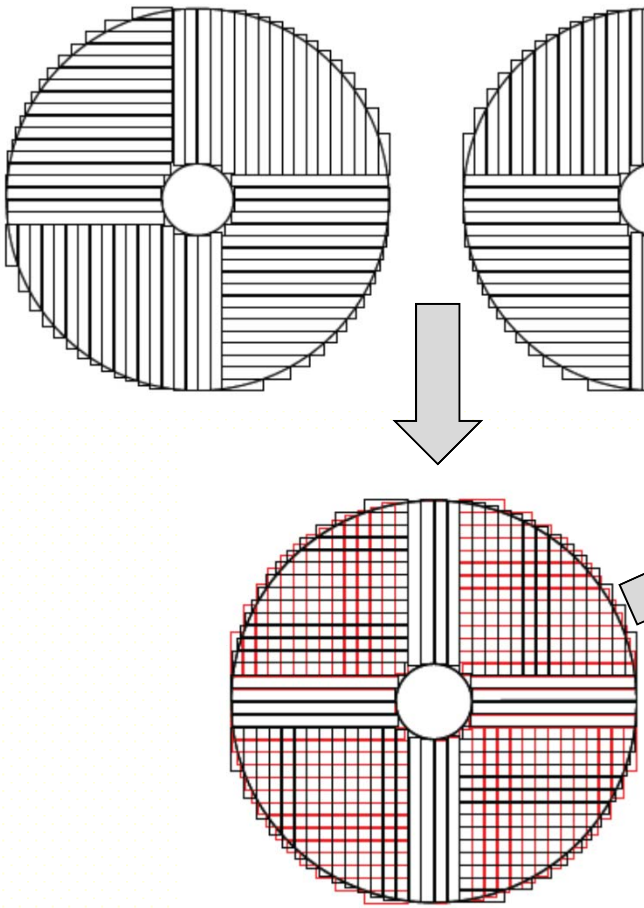
Modules overlap along X or Y depends on position

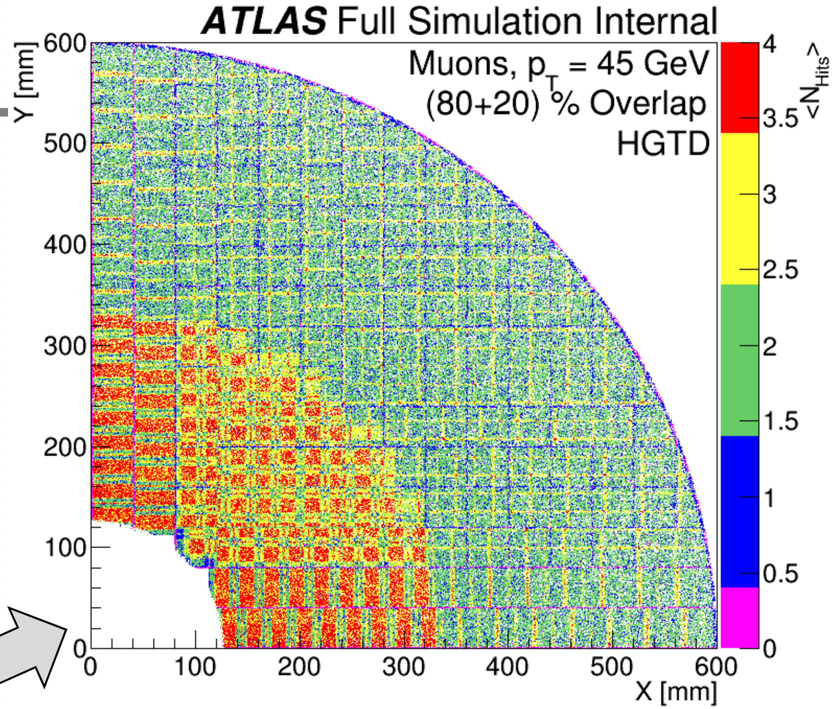
Still working on final design

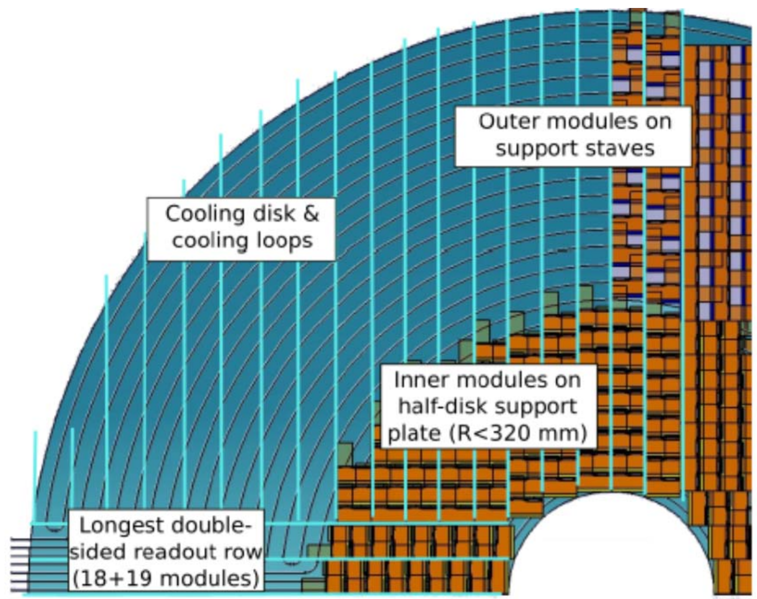


HGTD module and stave

First layer second layer

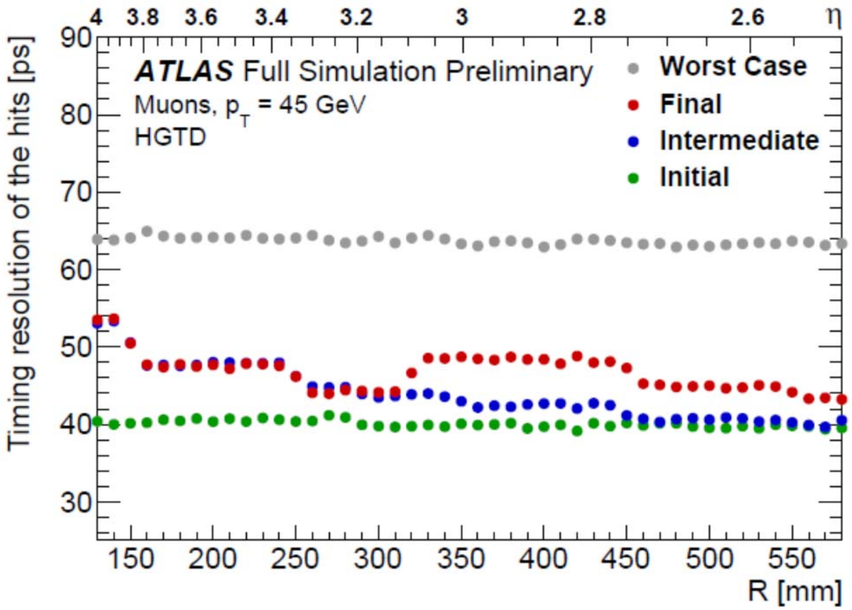




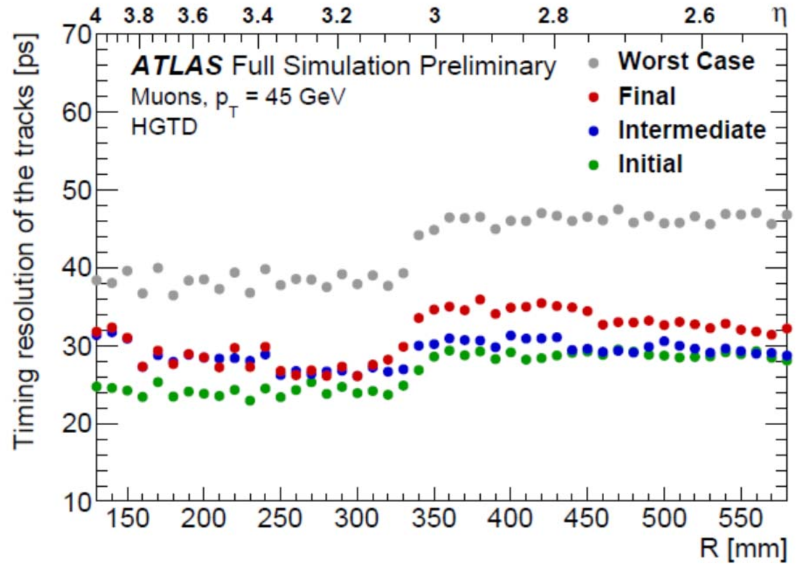


Summary expected time resolution

Sensor+electronics resolution per hit

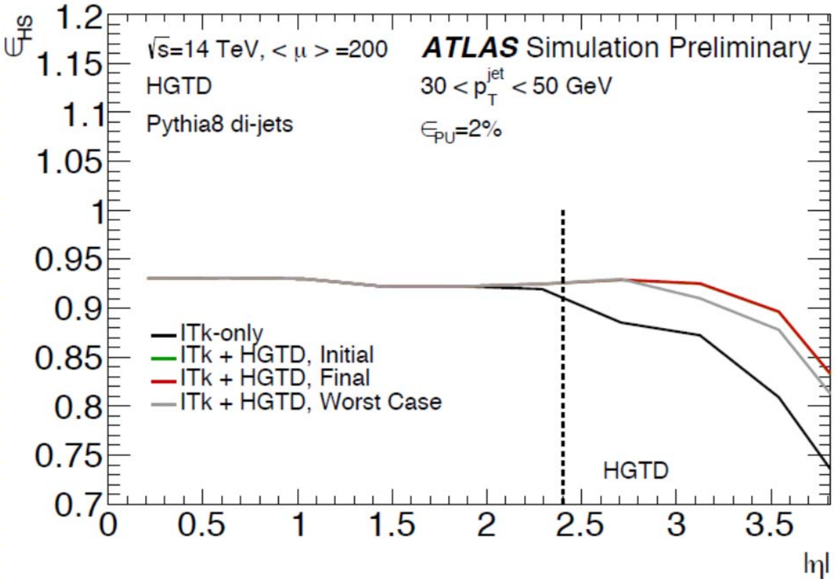


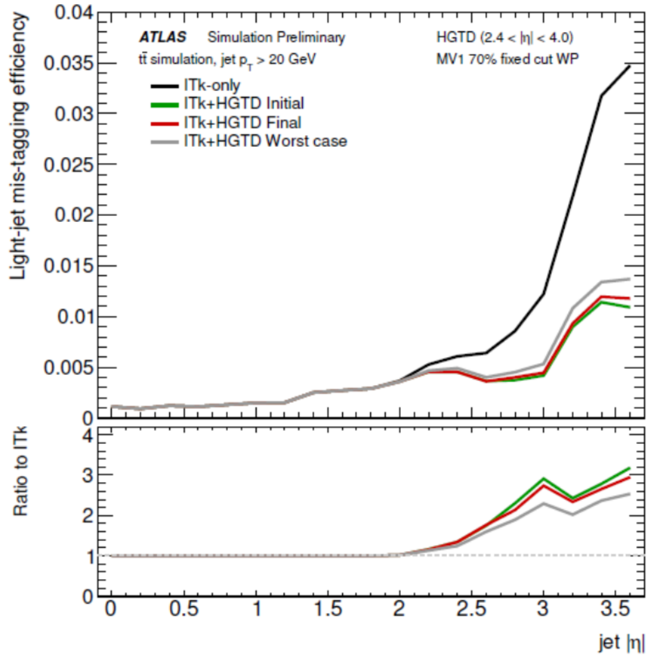
resolution per track

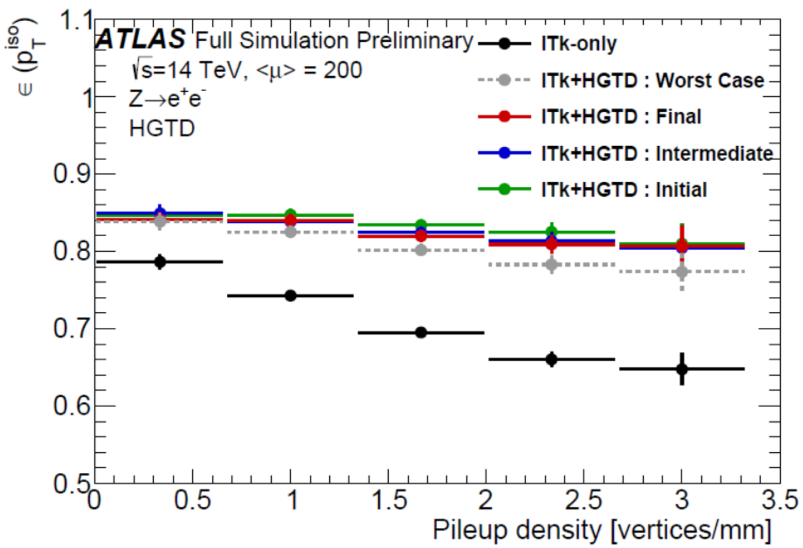


Modules at r < 320 mm replaced at middle of HL-LHC integrated luminosity
Compensate at inner radius time resolution by increasing number of hits.

Expected performance







Using HGTD in forward region :

- restore similar performance to central region (ITk only)
- small degradation w/ pileup density
  → Make more robust performance

Impact on physics channels (VBF Higgs, tH) expected about 10-15 %

Conclusion

Providing 30 ps per track resolution in the HL-LHC environment is quite challenging ….. but looks achievable.

R&D started in ATLAS about only two years ago but a lot progress/results achieved

Last review with LHCC on Technical Proposal this Monday

→ Hope green light in these days for a TDR by March 2019

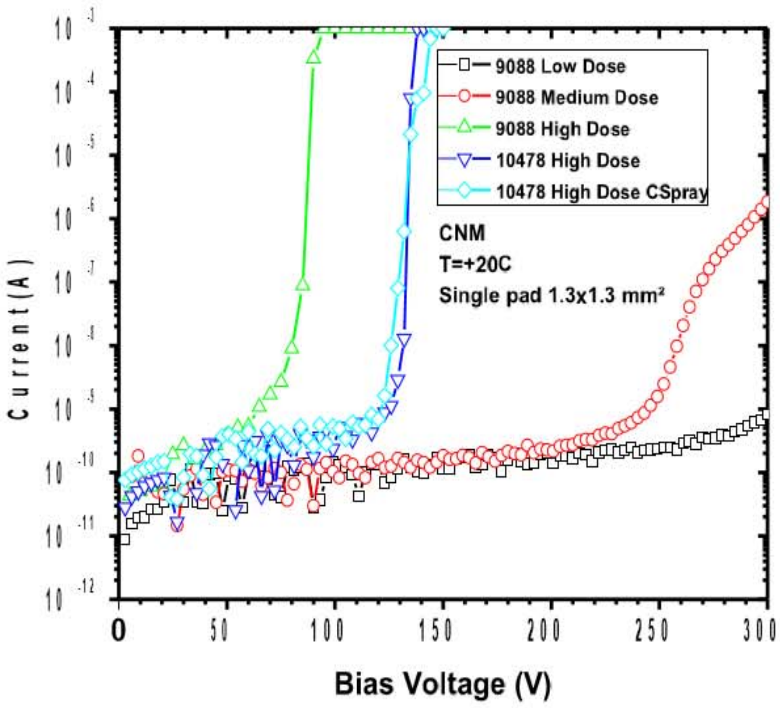
2018→2020 R&D to finalize HGTD design

2021→2024/25 : production / construction with stave 0 in 2021

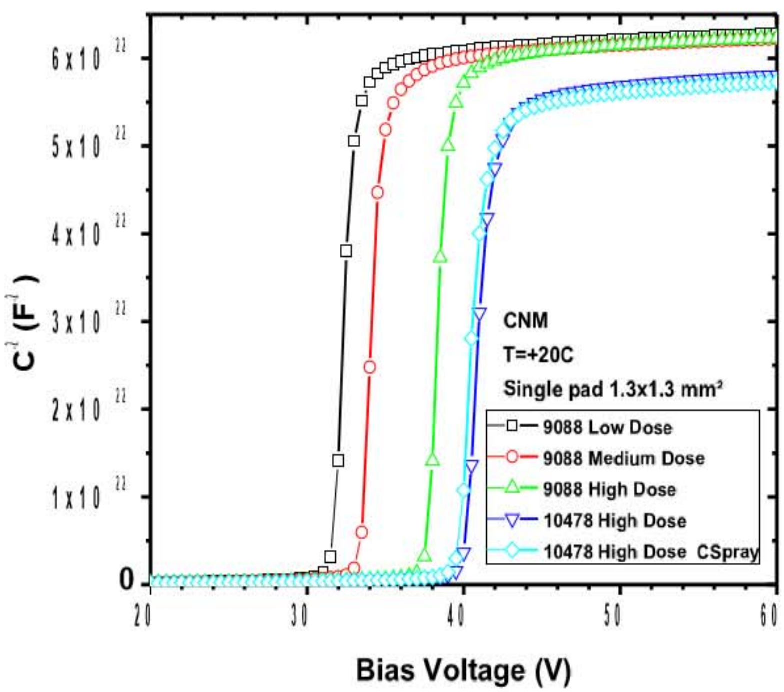
→ Installation in June/July 2025

BACK –UP

Sensor parameters : IV and CV curves

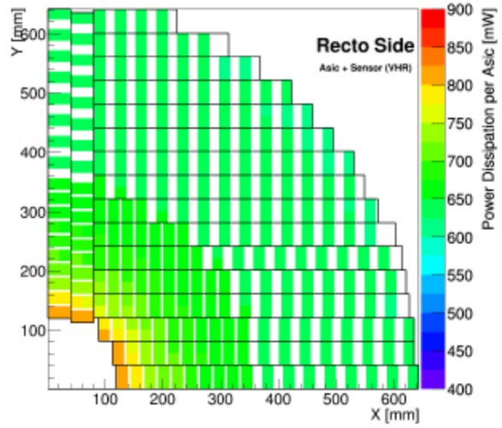


(a) Current vs Voltage



(b) Capacitance vs Voltage

Power dissipation



(a) Front view

Component	Nominal [µW]
Preamplifier	462
Discriminator+DAC	375
TDC TOT (10ns/40ps)	500
TDC TOA (2.5ns/20ps)	405
Local Memory	920
Total Pixel	2666

Table 11: Single pixel average readout power consumption. For the TDC and local memory (full buffer option), a 10% occupancy factor is applied.

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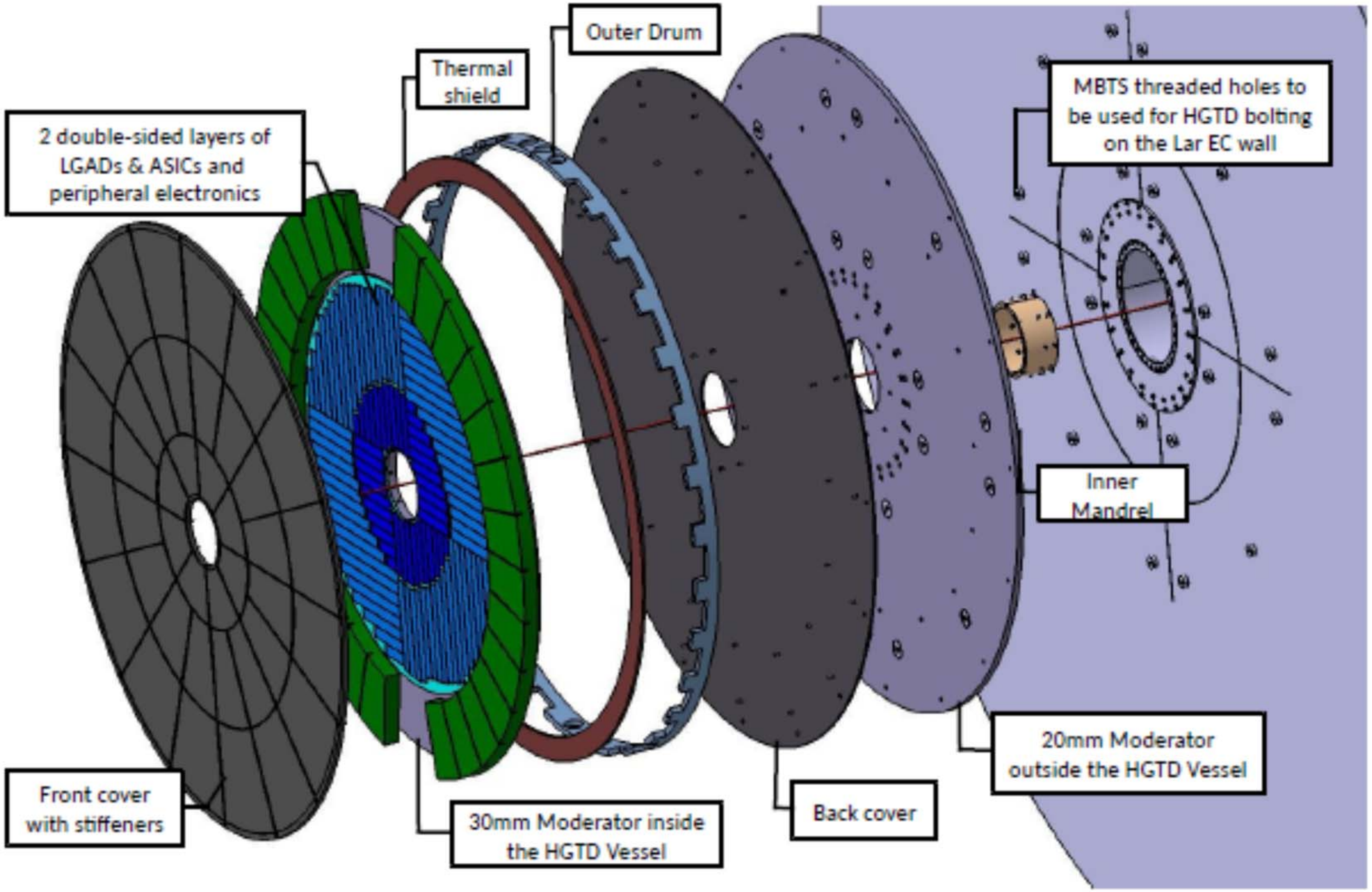
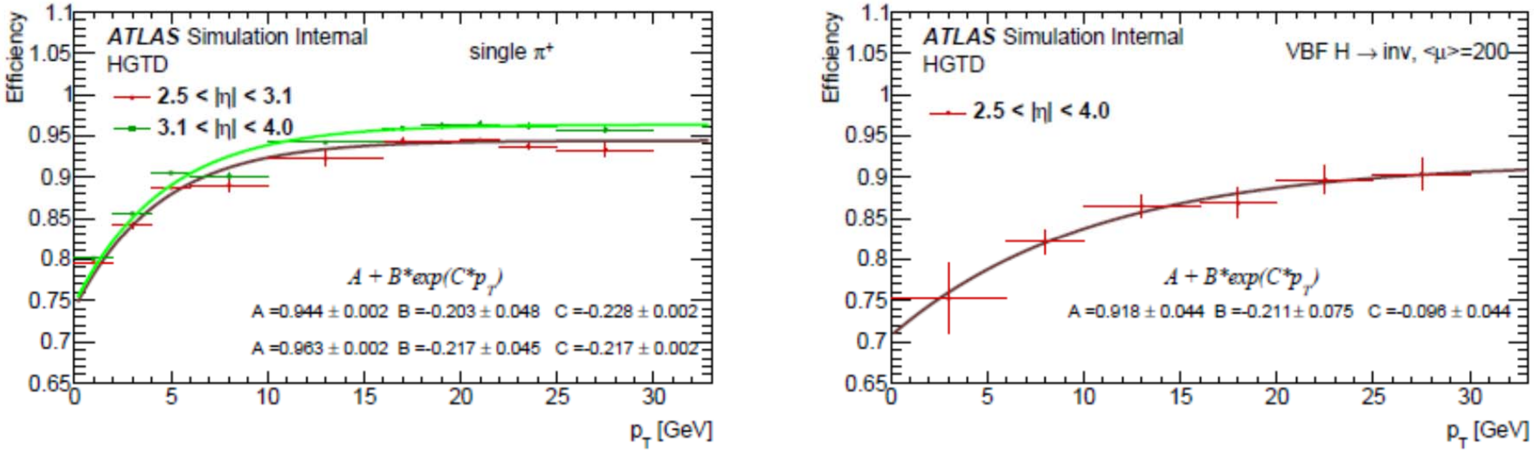
Component	Power consumption	Total [kW]	Maximal [kW]
Sensor	< 30 mW/cm^2	1.9	1.9
ASIC	<175 mW/cm^2	8.5	12.8
Flex cable	< 100 mW/flex	0.5	1.1
HGTD cold vessel heaters	75 W/m^2-175 W/m^2	0.33	0.33
EC calorimeter cryostat heaters	120 W/m^2, 50% up to R = 1600 mm	< 0.6	0.6
Peripheral on-detector electronics	dominated by DC/DC converter	3.25	4.9
Total for CO_2 cooling		15.1	21.6

HGTGD exploded view



Track matching efficiency



(a) Efficiency for matching tracks to at least one HGTD pixel. (b) Estimated efficiency for assigning the correct time to tracks.

Inter pad distance (fill factor)